Improving The Flatness Of Microdisplay Backplanes Using Chemical Mechanical Polishing

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MM

For my father

Acknowledgments

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Of course the production of a thesis is only a small part of any Ph.D. An equally important one is the friends which are made on the journey. I have been fortunate for my time at Edinburgh to meet some people who have made the time here very enjoyable, Georg, Chris, Kris, Dave, Vidar, Mark and Neil, to name but a few.

Abstract

Applications using liquid crystal on silicon (LCoS) spatial light modulators (SLM) demand a high level of device flatness. The overall backplane and individual mirror flatness directly influences SLM optical quality in a number of interrelated ways. They affect the liquid crystal (LC) cell gap uniformity, optical efficiency and LC alignment characteristics directly. In turn, the LC thickness variation and alignment quality affects device contrast ratio. The final cell gap uniformity, and LC alignment quality are also influenced by surface morphology, and by the chemistry of the surface over which the LC flows during cell filling. It is therefore critical to minimise the surface morphology and have a good understanding as to the LC's interaction with the surface over which it flows. Chemical mechanical polishing (CMP) can be used to increase device flatness and reduce the problems associated with surface morphology.

A technique to remove the layout and process dependent surface topography using CMP has been investigated. Problems were initially encountered due to the presence of the large, feature dense, pixel array. These were overcome by the development of a novel pre-CMP dielectric etch step, resulting in a greatly improved post-CMP dielectric uniformity and a sub-nanometer RMS surface finish.

Conventional planarisation techniques leave the mirrors standing proud of the surrounding dielectric surface. Two methods of reducing this mirror step-height have been compared, namely mirror damascene and via-damascene. The mirror-damascene method resulted in mirrors that are co-planar with the dielectric surface. While this improved the LC flow uniformity during cell filling, it introduced new concerns such as mirror dishing and array erosion.

A more attractive technique is that of via damascene which produces vias that are level with the dielectric surface. This approach allows the deposition of thin high quality aluminium mirrors. Initial problems were encountered with via dishing and CMP induced dielectric degradation; both of which were addressed using a post-damascene dielectric buff.

This thin mirror technique greatly reduces the surface topography induced LC flow front aberrations, but does not completely remove them. To further improve the LC fill characteristics a novel trench fill technique has been developed. This removed the inter-mirror trenches completely and resulted in virtually no LC flow front aberrations.

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Abbreviations

AFLC	Anti-ferroelectric liquid Crystal
AFM	Atomic Force Microscope
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
CRT	Cathode Ray Tube
CVD	Chemical Vapor Deposition
DI	De-ionized
DLP	Digital Light Processing
DMD	Deformable Mirror Device
DOF	Depth Of Focus
EA	Electrically Addressed
ECR	Electron Cyclotron Resonance
EMF	Edinburgh Microfabrication facility
FLC	Ferroelectric Liquid Crystal
GLV	Grating Light Valve
ITO	Indium Tin Oxide
LC	Liquid Crystal
LCD	Liquid Crystal Display
LCoS	Liquid Crystal over Silicon
MEMS	MicroElectroMechanical Structures
MINDIS	Miniature Information Display System
NLC	Nematic Liquid Crystal
PECVD	Plasma Enhanced Chemical Vapor Deposition
rf	Radio Frequency
RIE	Reactive Ion Etch
RA	Roughness Average
SEM	Scanning Electron Microscope
SIFT	Self-aligned Insulator Filled Trench
SLIMDIS	Silicon Liquid crystal Miniature Display System
SLM	Spatial Light Modulator
SRAM	Static Random Access Memory
SSFLC	Surface Stabilised Ferroelectric Liquid Crystal

1. Introduction

In the modern society the ability to manipulate information is becoming increasingly essential, including both the input and output of data. While the capability to process information has increased dramatically over the past four decades or so, the ability to visually access this information has lagged somewhat behind. The cathode ray tube (CRT) has been, and still is, the technology of preference for many types of information displays. The CRT offers high image quality, high image refresh rates, large viewing angle, is an established technology and is very cost effective. This technology does, however, have several drawbacks. When used to produce larger images they are relatively large and heavy (a Sony 32" FD TV weighs nearly 80kg) and require high drive voltages. A new breed of displays has recently begun to appear on the market, called microdisplays or spatial light modulators (SLMs). An SLM is a device which applies a spatially controlled modulation to an incident wavefront. SLMs are small, usually having an active display area less than 50mm in diagonal. These display engines are lighter in weight, smaller and require less power than CRT type displays. They can either be viewed directly (e.g. head-mounted systems) or can be used in projection systems to produce large images several meters in size.

SLMs are also more versatile than CRTs in that they cannot only be used as display engines but also have other applications. These include coherent light systems, such as, optical crossbar switches[1], reconfigurable holograms and optical correlators[2]. These non-display applications are becoming increasingly important as the world switches from electrical information to optically transmitted information. SLMs not only have the ability to route the optical signal but also to process that information.

Over the years many different SLM technologies have been reported and many types of modulation technology employed[3]. Among these are electro-optic[4,5] and magneto-optic[6], but the two most commonly used methods, for display applications[7], are Liquid Crystal over Silicon (LCoS) and mechanical effects or deformable mirror devices (DMD). These methods modulate a wave front in such a way as to create an image, e.g. mechanically or by the use of a liquid crystal 'shutter'. Table 1-1 lists these two common types of display technology and some of the manufactures that have adopted them.

Basic Technology	**Optical Imaging Technology**	**Representative Companies/Institutions**
MEMS MicroElectro-Mechanical Structures	Grating Light Valve Diffractive (GLV)	Silicon Light Machines
	Deformable Mirror Diffractive (DM)	Hertz Institute
	Digital Mirror Display, Reflective (DMD)	Texas Instruments
LCD	Ferroelectric LC Reflective (FLC)	Displaytech, MicroPix
	Bifringent Nematic Reflective (LCD)	Spatial Light
	Bifringent Nematic Diffractive (LCD)	MicroDisplay Technology
	Twisted Nematic Transmissive (LCD)	Kopin
	Twisted Nematic Transmissive (LCD)	Seiko-Epson, Sarif, Sharp, Sony
	Polymer Dispersed Reflective (PDLC)	Raychem/Hitachi, National Semiconductor

Table 1-1 Different display technologies and associated manufacturers who have adopted them[8]

1.1.1. MicroElectro-Mechanical Systems

MicroElectro-Mechanical Systems (MEMS) apply modulation to the incoming light by means of electrically addressed movable mechanical mirrors[9]. Probably the best known of this type of device is the Texas Instruments (TI) digital light processing (DLP) deformable mirror device (DMD), Figure 1.1

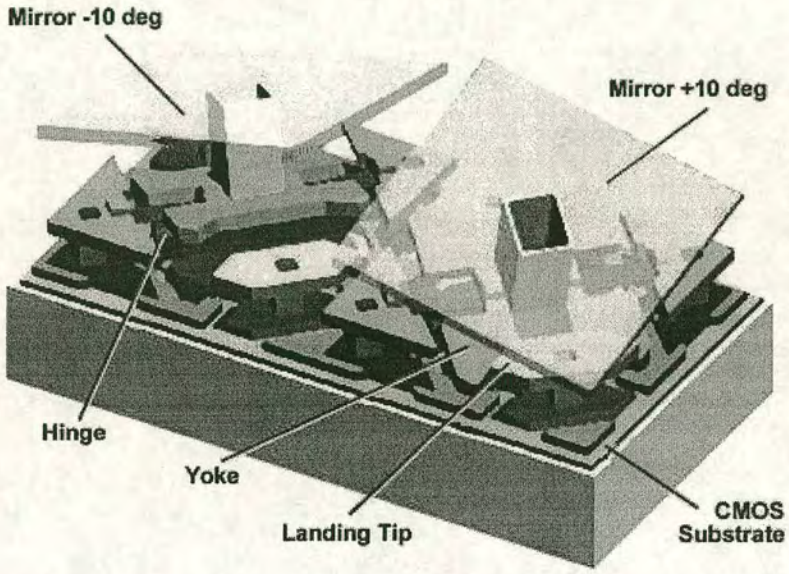


Figure 1.1 Schematic showing two mirrors of the Texas Instruments deformable mirror device (DMD)[10]

The TI Digital Light Processing technology, the DMD, is a Static Random Access Memory (SRAM) chip with an array of 508,000 (848 x 600) hinged, microscopic mirrors attached to its upper surface. Electro-static forces are used to deflect the reflecting elements and this deflection produces a direction change on the reflected light. Each mirror is equivalent to a single pixel in the projected image. A colour image is generated by the relative amount of time each mirror is in the 'on' or 'off' position when red, green or blue light shines on it determines the hue and shade of the pixel it generates.

A slightly different approach is taken by Silicon Light Machines, Figure 1.2 shows a schematic of their Grating Light Valve (GLV) technology.

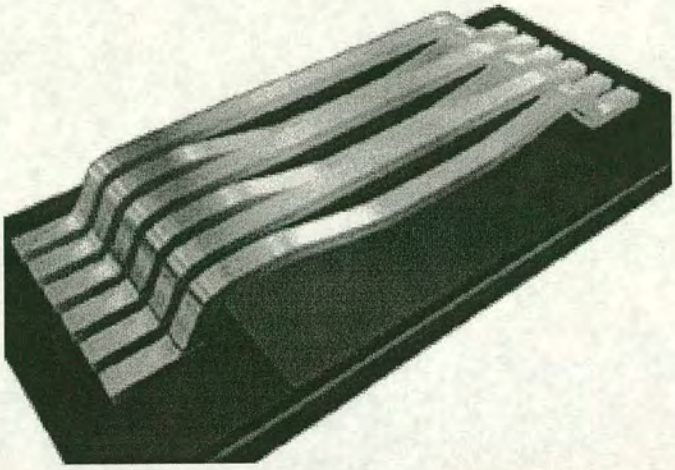


Figure 1.2 **Schematic of a small portion of a Silicon Light Machines Grating Light Valve (GLV) deformable mirror device (DMD)[11]**

To create a GLV device, MEMS techniques are used to form a 1-D of array of pixels on the surface of a silicon chip. Each of these pixels is made up of multiple ribbon-like structures, which can be deflected up (or down) by controlling electrostatic forces.

Each of the GLV arrays includes 1080 active pixels that correspond to a single vertical column of data from a 1920x1080 image. The modulated light is combined through a dichroic assembly and directed through a standard projection lens. A galvanometric mirror scans the image horizontally, such that each GLV pixel paints one row of colour channel data for each scan refresh.

Although this type of MEMS technology is used to produce SLM type devices it does have several technical disadvantages:

1 The device is not particularly mechanically robust

2 It is difficult to manufacture

3 It contains complex mechanical mechanisms

4 Not only the flatness but also the alignment of the individual 'free standing' mirrors is critical for device performance

1.1.2. Liquid Crystal On Silicon

In devices which use liquid crystal as the light-modulating medium the LC is placed in direct contact with the silicon circuitry. The circuitry then acts as both mirror and drive electronics. Figure 1.3 illustrates a typical layout of such a device.

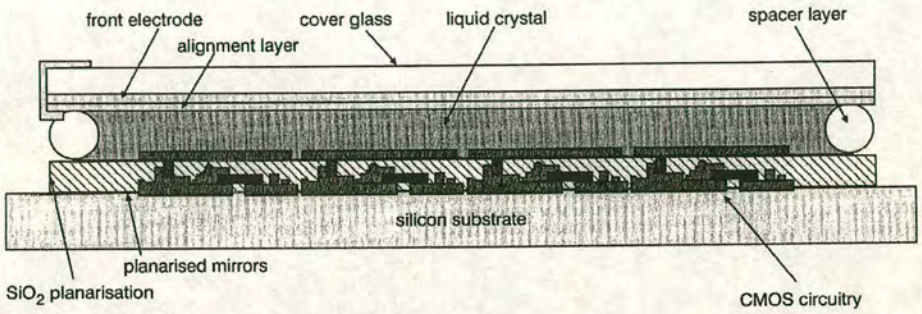


Figure 1.3 Schematic cross-section of LCoS type reflective SLM

LCoS SLMs were have been developed at the University of Edinburgh since the mid-1980's[12]. Since then, although the basic technology has remained much the same, many advances and improvements have been made. Perhaps the most important being the development of sophisticated techniques for post-processing of the silicon backplane. New LC materials, such as surface stabilised ferroelectric (SSFLC) and anti-ferroelectric (AFLC) are also beginning to be used in these LCoS devices. These new materials are, however, generally more difficult to align than other types of LC placing greater demands on post-processing methods.

In LCoS display applications the SLM is usually used in the reflective mode. A schematic of an SLMs operation can be seen in Figure 1.4 and a typical display viewing arraignment in Figure 1.5.

LCoS SLM pixels can be addressed using two main methods, electrical and optical addressing. In electrical addressed (EA) LCoS SLMs the switching of the pixel is via an electrical trigger. This work concentrates on the electrical addressed type of LCoS SLM.

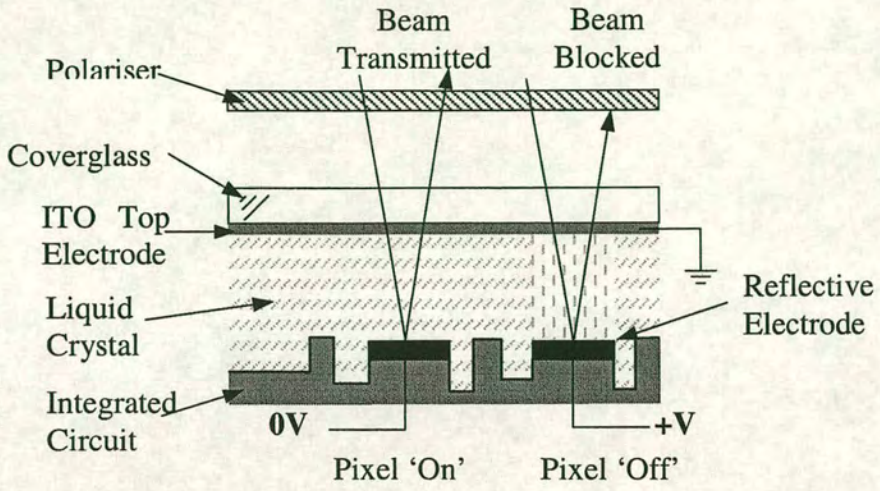


Figure 1.4 **Schematic, showing 2 pixels, of generic reflective SLM operation**

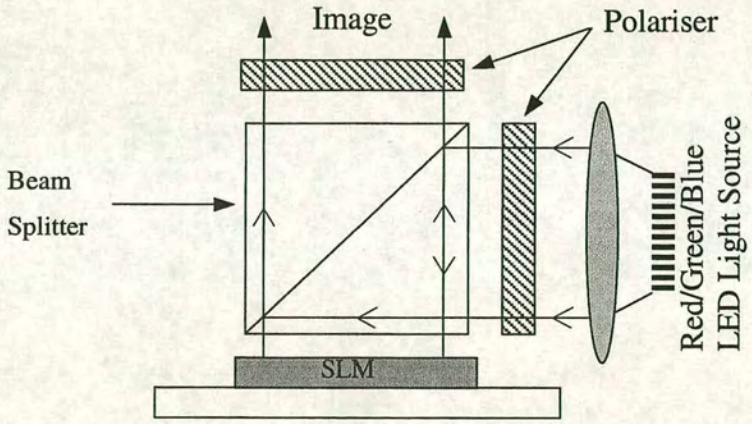


Figure 1.5 **Typical viewing arrangement of LCoS SLM in a display application**

Since the early days many sizes and configurations of LCoS SLM have been designed and manufactured, within the University of Edinburgh Table 1-2.

Device	Mirror Pitch/ Size	Display size/ Chip size	Frame Rate	Comments
16 x 16	200μm 100μm x 100μm	3.2mm x 3.2mm 7mm x 7mm	5Hz	SRAM nMOS[13]
50 x 50	72μm 45μm x 44μm	3.5mm x 3.5mm 7mm x 7mm	60Hz	SRAM Twisted Nematic LC[14]
176 x 176	30μm 22μm x 14μm	5mm x 5mm 10mm x 10mm	1kHz	DRAM Planarised[15]
64 x 64	80μm 45μm x 45μm	5mm x 5mm 10mm x 10mm	3kHz	DRAM High Voltage (± 25V)
256 x 256	40μm 18μ x 18μm	10mm x 10mm 14mm x 14mm	4kHz	SRAM Planarised[16]
512 x 512	20μm 18μ x 18μm	10mm x 10mm 14mm x 14mm	25kHz	DRAM Light Baffle layer[17]
1024 x 1024	12μm 10μm x 10μm	12mm x 12mm 14mm x 14mm	5kHz	DRAM 'SLIMDIS'[18]
1280 x 1024	10μm 8.4μm x 8.4μm	13mm x 10mm 14mm x 14mm	25kHz	DRAM 'MINDIS'[19]

Table 1-2 Summary of LCoS SLM's designed at the University of Edinburgh

1.1.3. Liquid Crystal

Obviously liquid crystal plays a key role in the operation of a LCoS SLM. As this thesis is primarily concerned with post-processing methods only a brief discussion will be entered into regarding LCs. However, it is useful to have a basic understanding of their optical properties and their use in displays.

Liquid crystals are materials that can exist in an intermediate state between a liquid and solid state. LC materials generally have several common characteristics. Among these are a rod-like or disk-like molecular structure, rigidness of the long axis, and strong dipoles and/or easily polarisable substituents. The distinguishing characteristic of the liquid crystalline state is the tendency of the molecules to behave like a liquid but still have a long range order. Each molecule tends to point along a common axis, called the director. This is in contrast to molecules in the liquid phase, which have no intrinsic order, or in the solid state where molecules are highly ordered and have little transitional freedom. The characteristic orientation order of the liquid crystal state is between the

traditional solid and liquid phases and this is the origin of the term mesogenic state (of intermediate form) used synonymously with the liquid crystal state.

The result of LCs being composed of individual dipole molecules is that, under the influence of an electric or magnetic field, they can be forced to rotate. Another key element is the LC's ability to rotate plane polarised light. If polarised light passes through an LC cell, of the correct thickness, it is rotated through 90°. If a polarising filter is placed to intercept this transmitted light it can be made to block the light, depending on the angle of polarisation of the impinging light. This polarisation angle is a function of molecule position and hence a function of whether an electric or magnetic field is applied.

There are different types of LC available for the manufacture of LCoS SLMs, and three are listed in Table 1-3 along with some of their main characteristics.

LC Type	Modulation	Drive	Bistable	Speed	Technology	Alignment
Nematic	Grey Scale	Analogue	No	Slow (ms)	Well Established	Relatively Easy
FLC	Binary	Digital	Yes	Fast (μs)	Less well Established	More demanding
AFLC	Grey Scale	Analogue	Tri-state	Fast (μs)	Emerging	Unknown at present

Table 1-3 Table showing attributes of different LC types.

SSFLC and AFLC based devices offer higher switching speeds (over nematic based devices), have a larger viewing angle and are bi-stable. They are, however, more difficult to align. This places greater demands on post-processing techniques in order to produce flatter and smoother backplanes.

1.1.4. LCoS SLM Performance, The Problems

Some of the major performance indicators for spatial light modulators (depending upon application) are listed in Table 1-4

	Attribute	Optical Processing	Optical Switching/Routing	Displays
1	Pixel Count	High	Moderate	Very High
2	Frame Rate	Very High	Moderate	High
3	Throughput Efficiency	High	High	High
4	Contrast Ratio	Very High	Very High	High
5	Phase Flatness	Extremely High	Very High	High
6	Manufacturing Uniformity (SLM to SLM)	Very High	Very High	High
7	Size	Moderate	Moderate	Low
8	Weight	Moderate	Moderate	Low
9	Cost	High	High	Very Low

Table 1-4 Summary of the more important LCoS attributes for different applications

Attributes 3,4,5 and 6 can all be enhanced with improved post-processing techniques

For a reflective LCoS SLM technology used in display applications flatness is a key factor at all scales from macroscopic to microscopic. It is generally the case that, if no special care is taken, a silicon backplane will show a degree of 'un-flatness' at all scales due to the following causes:

1 **Backplane**: Chip bow causes distortion of a reflected wavefront and large scale variations in FLC thickness and alignment, again resulting in noticeable contrast variations which are manifested as colour fringes in microdisplays[20] (Figure 1.6 *a* and *b*)

2 **Pixel**: Circuit topography scatters light and causes variations in the director alignment of the liquid crystal layer which show up as sharp variations in contrast in a finished SLM (Figure 1.6 *c* and *d*)

3 **Sub-micron**: Metal granularity can cause scattering of incident light[21] (Figure 1.6 *e* and *f*) and seed alignment defects in the LC

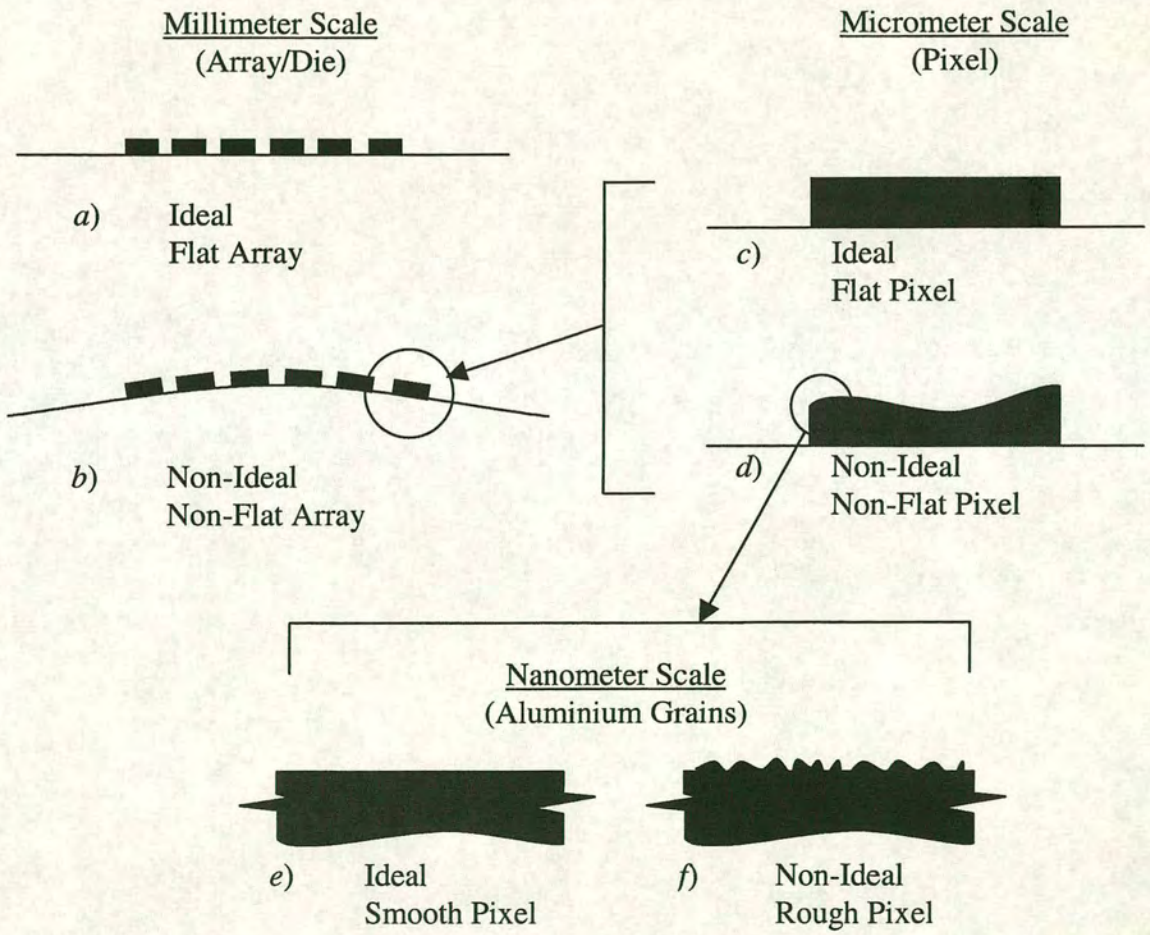


Figure 1.6 **Illustration of different degrees of 'un-flatness' for LCoS SLM**

Die Warp

The flatness of the die is important for microdisplay optical quality. During processing, the wafer (and hence each individual die) undergoes many process steps. During some of these steps, mainly deposition and heat treatments, stresses are induced into the wafer. On dicing, some of theses stresses can be released and die warp can result. This warp makes it difficult to accurately, and reliably, set the LC cell gap thickness. Figure 1.7 shows a typical amount of die warp found in a fully processes 512^2 device after dicing. The resultant non-uniform cell gap results in colour and contrast variations across the final image, as shown in Figure 1.8

The causes, and a possible remedy, of this die warp will be discussed more thoroughly in Chapter 10. However, it must be realised that all surface planarisation techniques are unable to remove this type of die warp.

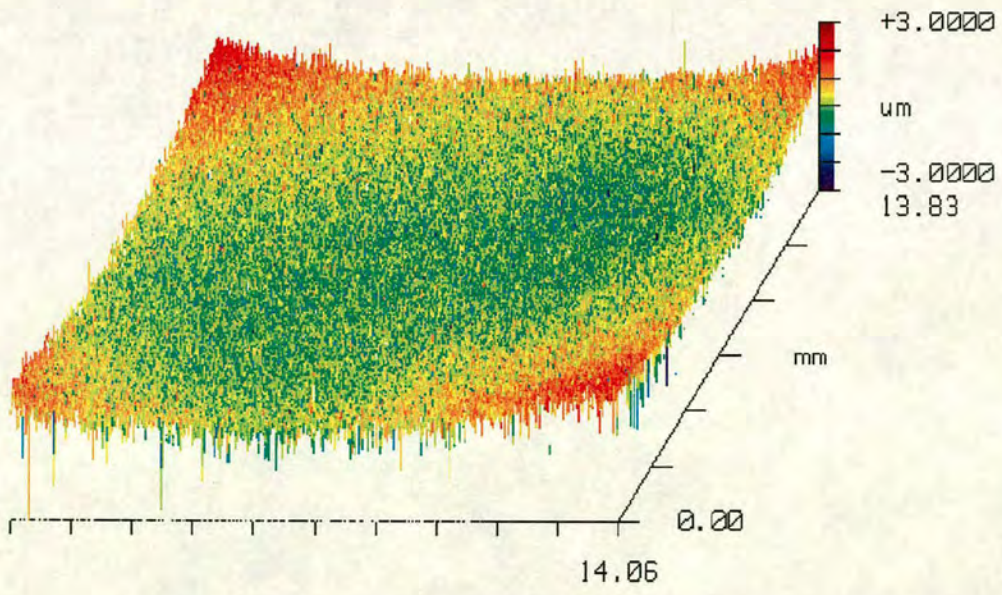


Figure 1.7 **White light interference image showing flatness of fully processed 512^2 device (die size is 14mm x 14mm and die warp is ≈2μm)**

Figure 1.8 **Image generated on SLIMDIS SLM showing colour and contrast variation as a result of (among other things) poor LC cell gap uniformity (Courtesy Mike Worboys GEC Marconi)**

Fill Factor

The mirror fill factor (FF) is the ratio of mirror area to non-mirror area, of the active region, and is defined in Equation 1-1

$$Fill\ Factor = \frac{Total\ Mirror\ Area}{Total\ Array\ Area} \times 100$$

Equation 1-1 Definition of Fill factor

As the mirror size continues to shrink so does the mirror FF, because of the necessity to maintain an inter-mirror spacing. This gap ensures that each individual mirror remains electricaly isolated. The only way to maintain the mirror FF is to have larger active areas with the same size mirrors.

1.1.5. Real Devices

SEM images of the 512^2 and MINDIS devices, as received from the foundry can be seen in Figure 1.9 and Figure 1.10.

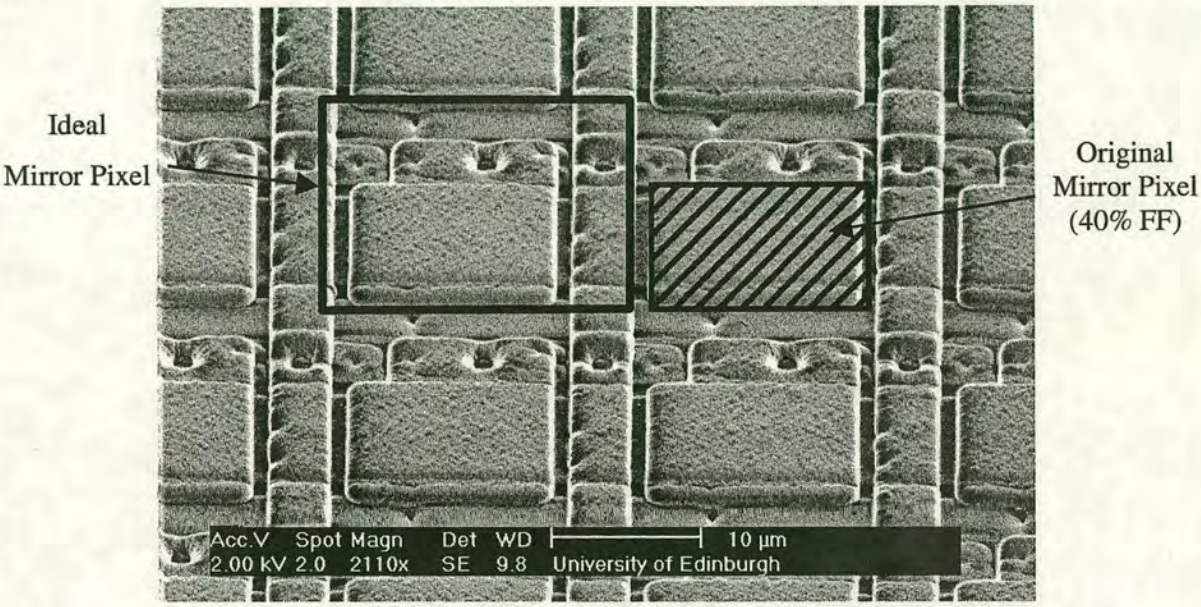


Figure 1.9 **SEM Image of 4 pixels of 512^2 device as delivered by the foundry (SEM image courtesy of D. Travis)**

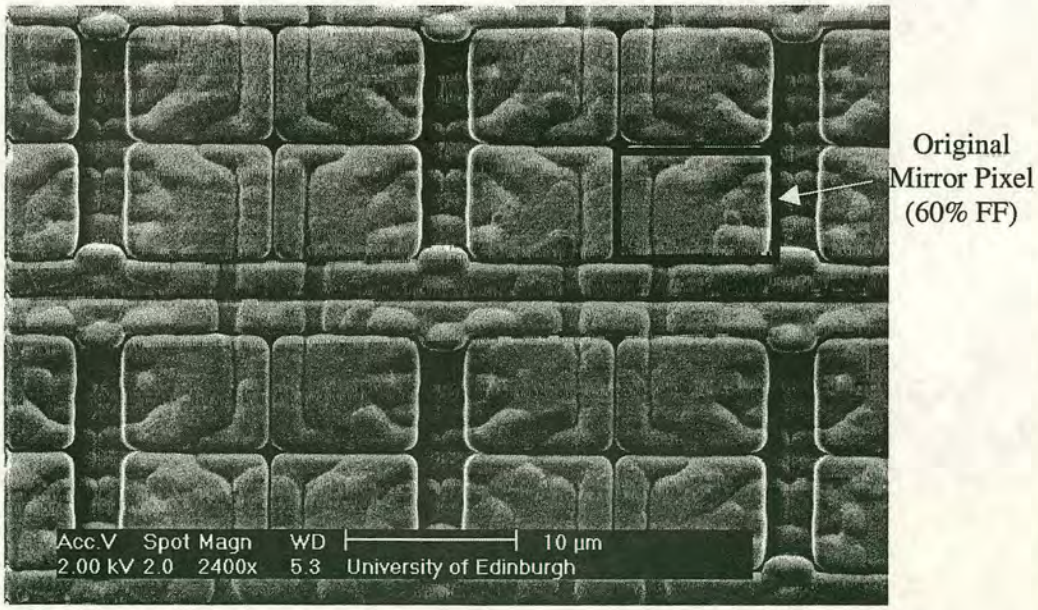


Figure 1.10 **SEM Image of 4 groups of 4 pixels of 'MINDIS' device as delivered by the foundry (SEM image courtesy of D. Travis)**

It can be observed that both the devices suffer from a relatively low mirror FF of 40% and 60% respectively. In addition to this the mirrors, particularly on the MINDIS device, are far from flat and their surfaces are rough.

Of course, none of these problems appear in isolation, they can, and do, occur together. A list of the problems and their possible effect can be see in Table 1-5.

Defect	Mechanism	Effect
Non Flat Mirrors	Increased light scattering	Loss of optical efficiency Loss of image brightness
	Variable electric field across LC	Spurious LC switching effects
Rough Mirrors	Increased light scattering	Loss of optical efficiency
Low Fill Factor	Low reflectance	Loss of optical efficiency
	Exposed drive circuitry	Spurious LC switching effects
Low Planarity	Difficulty in setting cell gap	Different optical path lengths Contrast ratio variations Coloured Fringing in display
	Variable electric field across LC	Spurious LC switching effects
	Poor LC fill dynamics	Poor final LC alignment Contrast ratio variations
Array step height	Difficulty in setting cell gap	Different optical path lengths
Die Warp	Difficulty in setting cell gap	Coloured Fringing in display Contrast ratio variations Loss of optical efficiency

Table 1-5 Table showing effects of non-ideal backplane

1.1.6. The solutions

Each problem does not have a unique solution but rather a combination of solutions:

1 The application of SiO_2 CMP techniques to reduce or remove circuitry induced surface topography and allow the deposition of 'flat' high FF mirrors

2 The use of metal damascene techniques to reduce or remove mirror topography

3 The use of 'thin mirrors' to improve mirror reflectivity and LC fill dynamics

4 The development of novel microfabrication techniques to improve the LC fill dynamics

5 The implementation of techniques to reduce die warp

1.1.7. Light Blocking Layer

If the device is to be used in a projection display system then it will be subjected to high levels of incident illumination. If the incident light penetrates into the underlying circuitry, by travelling between the pixel mirrors, it may lead to charge leakage in DRAM devices. To combat this problem another metal layer is placed between the mirror layer and circuitry in such a way as to block any direct path to the underlying circuitry, Figure 1.11

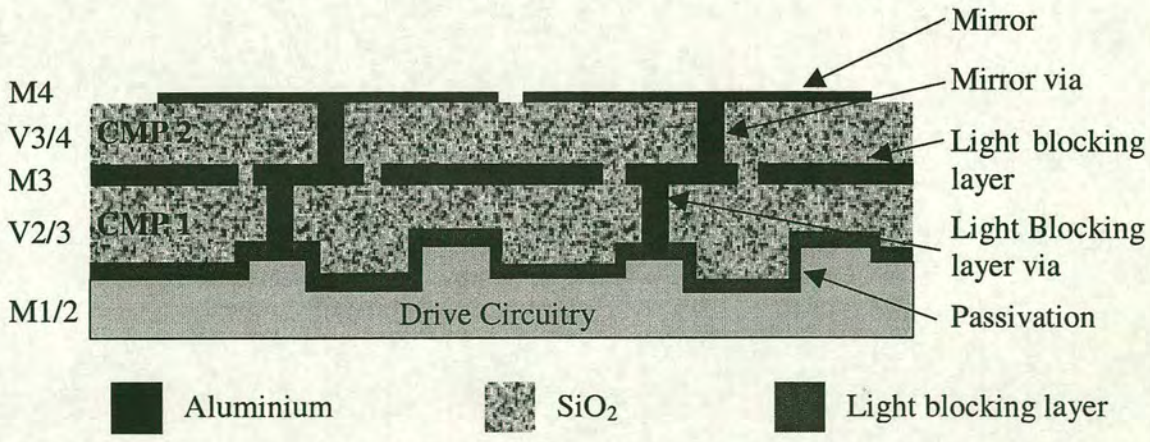


Figure 1.11 Schematic cross-section of 2 mirrors of a LCoS SLM incorporating a light blocking layer

1.2. Planarisation

The requirements, and reasons, for the dielectric planarisation of micro-displays are more demanding than those of integrated circuits (ICs). The technology is, however, identical. Chapter 2 explains why dielectric planarisation is now a necessary step in the production of ICs, in this section the motivations for LCoS dielectric planarisation will be discussed.

The planarisation of metals has also become critical for the production of integrated circuits, although for different reasons than those for dielectric planarisation, discussed in Chapter 5. Again, the motivations and requirements for metal damascene of micro-displays are different than those of ICs and are examined.

1.2.1. LCoS Display Dielectric Planarisation

Although the production of LCoS microdisplays will benefit by having its drive circuitry planarised, the main advantages come with the improvement in optical quality.

The optical quality of LCoS SLMs is a direct function of mirror surface smoothness and flatness and array/die flatness (Figure 1.6). The surface quality and flatness of the original mirrors, seen in Figure 1.9 and Figure 1.10, is poor. They also have a far from ideal mirror FF of 40% (512^2) and 60% (MINDIS). This poor original mirror FF results in low reflected light levels and possible spurious optical and electrical signals from the surrounding exposed drive circuitry. The area of LC which is 'switchable' is also a function of mirror FF, as these are also the LC 'drive' electrodes. The lower the mirror FF the lower will be the ratio of switchable to non-switchable LC area. This gives rise to a loss in final image contrast and brightness. Furthermore, because all the drive circuitry surrounding the mirror electrode is exposed to the LC, the current travelling along the address lines may also cause the LC to switch.

To increase the mirror FF it is necessary to deposit another mirror metal layer on top of the existing circuitry and pattern connections between the two. Although this would increase the mirror FF the resultant mirror would lie over the drive circuitry and would be far from flat. This would cause degradation in the optical performance of the device in a number of ways. The poor flatness would cause an increase in light scattering therefore a loss in the quantity of light returning through the optical system, resulting in a loss of image brightness and contrast.

Another problem associated with device non-planarity is that of LC filling and setting a uniform, and correct, LC cell gap thickness. As the LC is filled by capillary action the uniformity of the LC flow front will affect the final alignment quality. Any surface topography will disrupt the flow front and hence degrade the final LC alignment.

The LC requires the presence of an electric field to alter its orientation (switch). The strength of the electric field is a function of the distance between the two electrodes. If this distance varies so to will the electric field causing different LC response times and possibly a variation in contrast ratio, across the active display area leading to anomalous image effects. If the LC thickness is not uniform across the entire active display area it will also introduce different path lengths into the reflected light. This manifests itself as coloured fringes in the viewed image, due to different degrees of polarisation of the various wavelengths of light used to create the image, Figure 1.8

To reduce these problems it is necessary to post-process the as received devices. This entails using some type of dielectric planarisation to remove the surface topography. This allows the deposition of the final metal layer on to the smooth planar surface to create the mirrors. Unfortunately the final mirror metal thickness results in the mirror surface being approximately 1.6μm above the planarised oxide surface. This mirror step height causes problems associated with the LC filling causing a possible degradation in final LC alignment quality. To remove the mirror topography it is necessary to employ a further planarisation step, described in Chapters 7 and 8.

1.2.2. Dielectric Planarisation Methods

Many methods of planarisation have been developed. To compare these techniques several different metrics have been devised to assess the amount of planarisation achieved by any given technique. The method which seems to have gained most acceptance is shown in Figure 1.12.

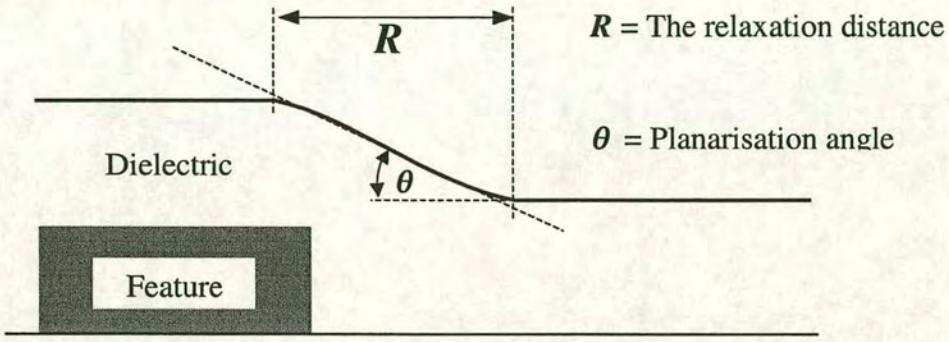


Figure 1.12 Quantitative definition of planarisation[22].

The planarisation relaxation distance, ***R***, is defined as the horizontal span of the tapered region. The angle between the taper and the x axis is defined as the planarisation angle θ. Further to this precise classification, the ability for a technique to planarise is usually defined as gap fill, local planarisation and global planarisation, Figure 1.13.

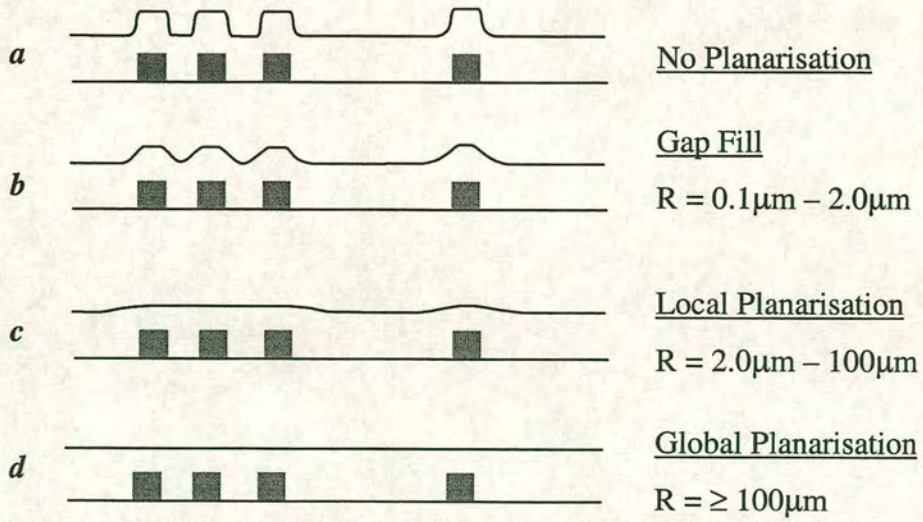


Figure 1.13 Schematic of Gap fill, local planarisation and global planarisation

There are many methods to planarise topography currently available[23], such as. ECR PECVD[24], deposition/etch[25], reflow[26], spin on glass[27], resist and etch back and CMP. These are listed in Figure 1.14 along with their ability to planarise.

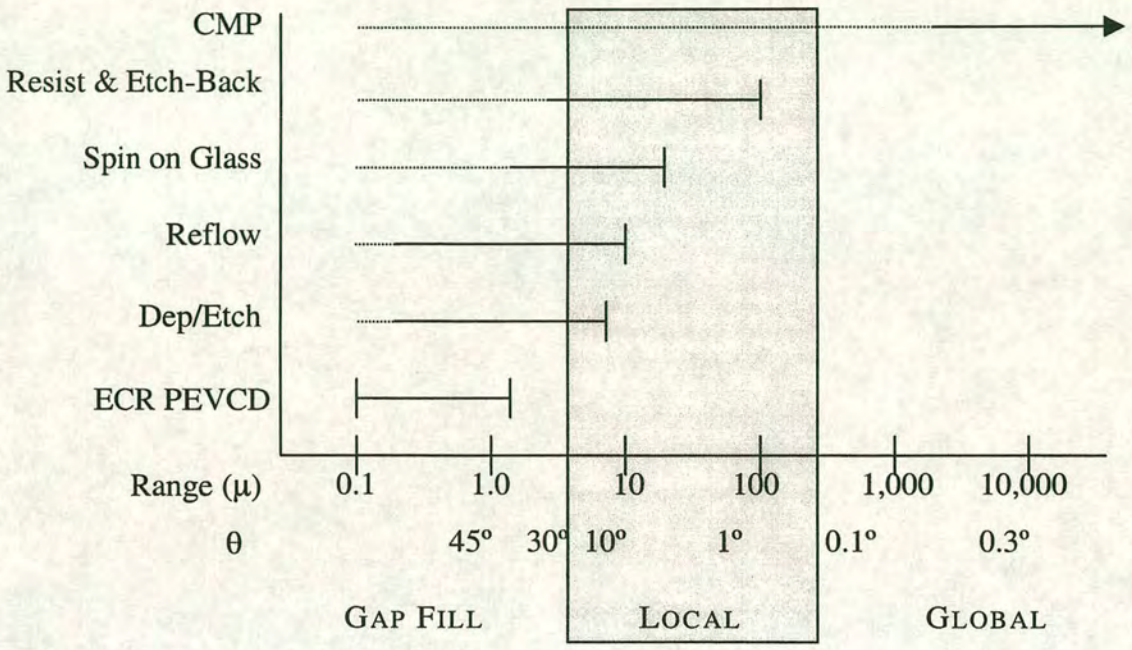


Figure 1.14 The range of planarisation for various processes

The planarisation of SLMs needs to be achieved on length scales of millimetres if not tens of millimetres. It is obvious from Figure 1.14 that the only technique to achieve this is CMP. Other techniques can give gap fill or local planarisation, although this would reduce the array topography it would not remove the overall array step height.

Although not of benefit directly, one method does go hand-in-hand with CMP is ECR PECVD. CMP is very good at removing surface topography over long distances but it has problems removing trenches because of the large amount of material needed to be removed. Furthermore to achieve total planarity CMP needs the underlying material to be free of voids and defects. Electron cyclotron resonance pressure enhanced chemical vapour deposition (ECR PEVCD) has the ability to fill trenches and produce void-free films.

1.2.3. LCoS Display Metal Planarisation

One of the problems in the manufacture of LCoS SLMs' is that of liquid crystal alignment quality. It is known that the LC alignment is a function of its fill dynamics and therefore any improvement in fill uniformity will have a beneficial effect on final LC alignment. The manufacture of SLMs, using conventional techniques, *a*, leaves the mirrors standing proud of the surrounding area by as much as 1.6μm and with a poor surface finish, Figure 1.15. This mirror thickness is necessary to ensure good via fill and hence good electrical contact to the underlying circuitry.

One problem with this method is that difficulties are created with LC filling, in the form of turbulence induced alignment defects caused by the LC flow over and around the raised mirror elements[28] This phenomenon has been termed "capillary pinning"[29]. This effect can be seen in Figure 1.15*b*, in which the LC (Merck E7) fill is from left to right, with the cell gap set at 3.1μm using spacer balls mixed within the cover glass adhesive. It can be seen that the LC flow front is far removed from the ideal linear shape. In addition the poor surface finish of the mirrors also contributes to the unsatisfactory LC fill dynamics, which is examined in more detail in Chapter 9.

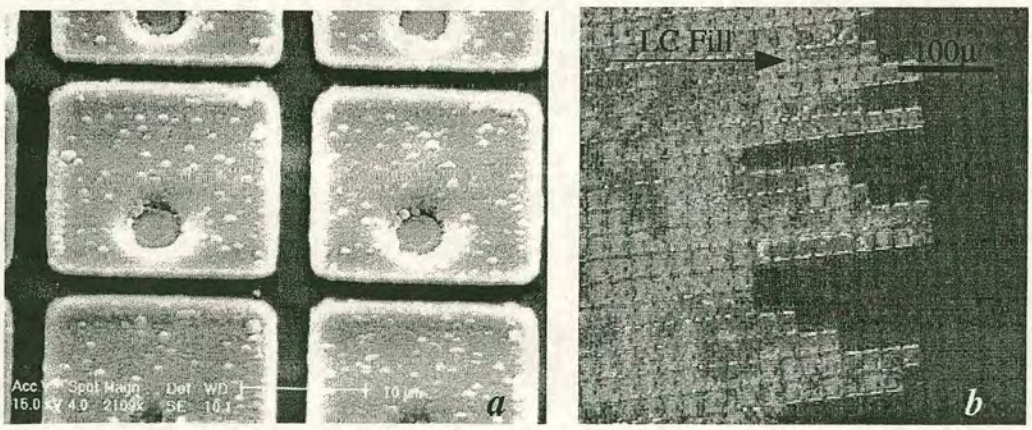


Figure 1.15 SEM image of 512^2 mirrors (a) and resultant LC fill flow front (b)

One way to overcome this problem is to manufacture mirrors whose surfaces are level with the dielectric insulating layer. O'Hara *et al*[30] suggested a damascene

technique may be used for the manufacture of LCoS SLMs. This would reduce the surface topography of the mirrors. Unfortunately it introduces new concerns such as array dishing, pixel dishing and scratching. These problems need to be overcome before this technique can be adopted for the manufacture of LCoS devices.

1.3. Aims and Thesis Outline

The main aim of this study has been to investigate ways to improve the quality of in house designed SLMs. A particular emphasis has been placed on the investigation and development of new CMP techniques for both dielectric and metal. The overall die flatness has also been studied and its causes investigated.

Throughout this study I have worked extensively on the 512^2 SLM. This is in main because there has been an ample supply of these devices and it is representative of most types of LCoS SLM designed at Edinburgh. Although all methods described in this thesis have been developed for this device it is expected that it will be relatively straightforward to transfer the techniques to other LCoS SLM designs.

This thesis covers three main areas.

Section 1 Chapter 2 to Chapter 4 describes the CMP of dielectrics and outlines a technique I have developed for the planarisation of the 512^2

Section 2 Chapter 5 to Chapter 8 describes the CMP of metals with a particular focus on aluminium. The development of both dual damascene (for the mirrors) and single damascene (for the vias) methods are described and the technologies compared.

Section 3 Chapter 9 investigates how the LC fill flow front dynamics can be modified by the use of a novel trench-fill technique.

Chapter 10 concludes the thesis with a summary of the relative merits of the techniques which have been developed during my Ph.D. study. It also highlights work which is in progress at the time of writing and comments on its relevance and possible outcome.

2. Dielectric CMP

The origins of dielectric CMP can be traced back to IBM in the early 1980's[31]. Like many revolutionary developments it appears to have been the result of a hallway conversation between Bill Guthrie, Bill Patrick and Charles Stanley. It all seems to have been quite casual, just one of those times when someone says "Hey I have this mad idea...". By the mid 1980's CMP was beginning to make the move out of the labs and into pilot production lines. All this time the development of CMP was a closely guarded IBM secret with little, if any, information leaving the company. It was not until 1988 that IBM began to share its knowledge with Sematech who, given sparse information, decided to run their own research and development program. By the early 1990's CMP came into the public domain and it was only then that it actually started to deliver what it had always promised, being a usable technology producing a useful product.

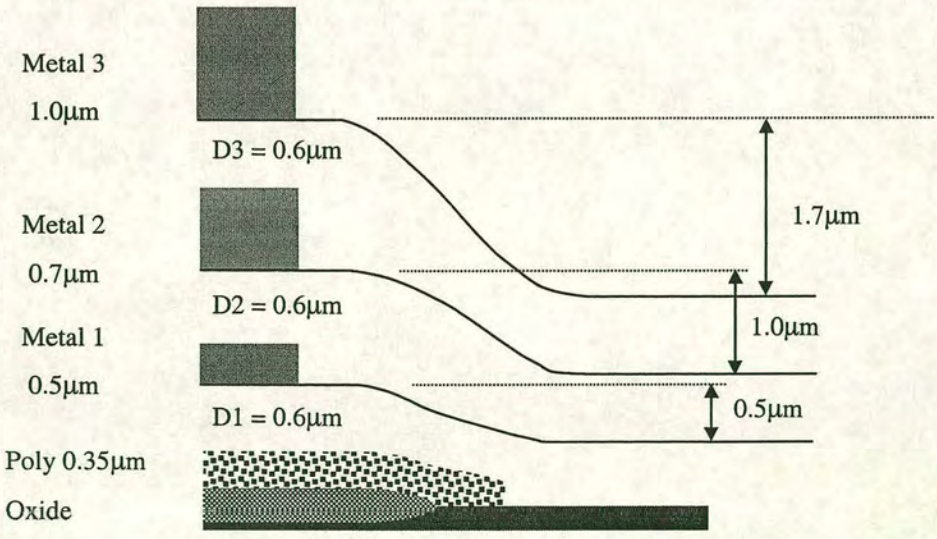


Figure 2.1 **Cross-sectional schematic of the build up of topography during manufacture of integrated circuits[32]**

The question as to why we need to planarise at all has many answers. For the electronics industry, for which the process was invented, the answers are simple Figure 2.1 shows how the surface topography can rapidly become very large during IC manufacture.

This surface topography causes four main problems:

1 Step coverage issues, Figure 2.2a

2 Depth of focus issues, Figure 2.2b

3 Different resist thickness, Figure 2.2c

4 Increased unwanted light scattering, Figure 2.2d

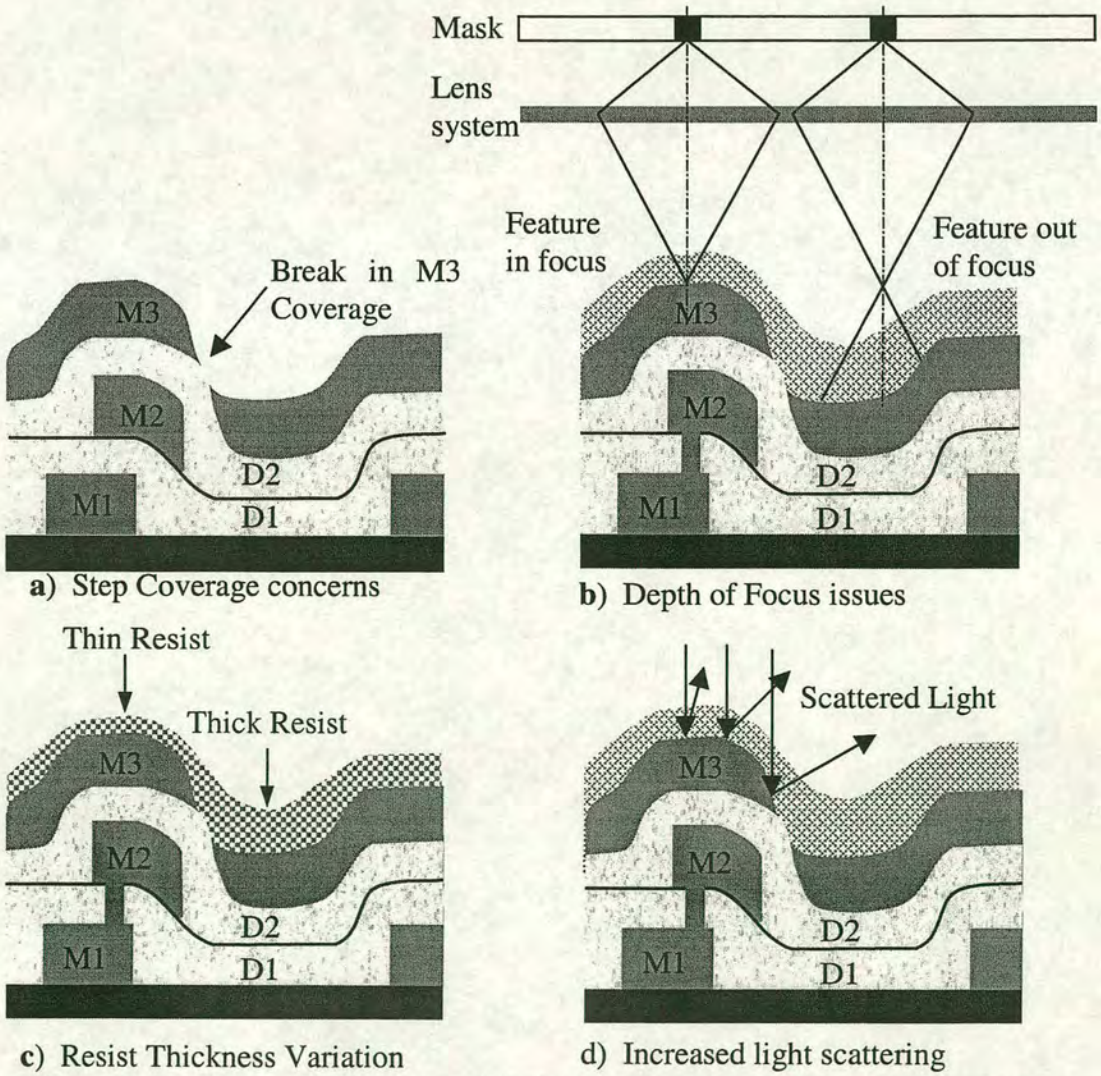


Figure 2.2 **Schematic illustration of the problems associated with surface topography**

Step Coverage

Step coverage concerns result from film deposition on a vertical wall being slower than on a horizontal area[33], Figure 2.2a. This causes the final deposited film to be of non-uniform thickness resulting in possible variations in the final interconnect thickness. This loss in crossectional area equates to a loss in current carrying ability which increases the vulnerability of the line to electronmigration induced failures as well as potential yield reduction. In extreme cases the step height can cause a break in the interconnect causing total device failure.

Depth of Focus

As the demands for smaller features continue the demands made on photolithography rise. As a result, modern steppers have a very small depth of focus (DOF)[34]. The DOF is the vertical distance in which the projected image is in focus, Figure 2.2b. The variation in the height of the topography is now exceeding the DOF, as a consequence the image is out of focus in some areas of the die, causing a degradation in the transferred image.

Resist Thickness

The surface topography causes the spun on photo-resist thickness to vary depending on the location on the die Figure 2.2c. The amount of light required to create an image on the resist is a function of resist thickness. This leads to some areas being under-exposed causing degradation, or even complete loss, of the transferred image.

Scattering

To define the pattern light passes through the resist and modifies it in such a way that makes it sensitive to the developer. When the light has passed through the resist it encounters the material beneath and is reflected back. If the surface is not flat this reflected light will be scattered, Figure 2.2d. The scattered light

reflected from the surface passes through the resist a second time, from below, causing unwanted exposed regions. On developing all the exposed areas are removed (for a positive resist) including the area exposed by the scattered reflected light. After etching this creates 'notches' in the feature, causing a degradation in performance.

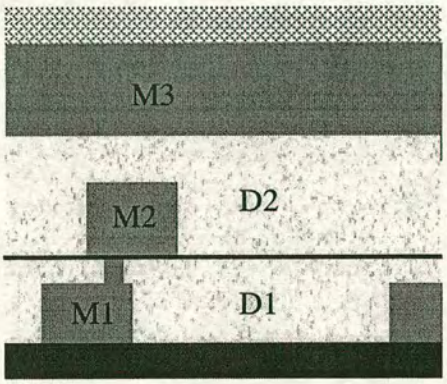


Figure 2.3 Schematic of section of (ideally) planarised circuitry

If the device is planarised the above problems can be removed or minimised. Figure 2.3 shows a section of a device that has been planarised after each dielectric deposition and it can be observed that it no longer suffer from surface morphology induced problems.

In the following sections both the material removal mechanism and CMPs' ability to achieve planarasiation will be examined.

2.2. Chemical Processes in Dielectric CMP

Most of the early work on dielectric CMP was derived from the glass polishing fraternity, as most dielectrics have glass like properties. Glass lenses have been produced for hundreds, if not thousands, of years without any true understanding of the mechanisms involved in material removal. It was not until the advent of CMP that much of the empirical information was re-visited and a more fundamental explanation sought.

For a more in-depth discussion into the physical mechanisms involved in dielectric CMP the reader is advised to read the papers by M. Tomozawa[35] and L.M. Cook[36].

2.2.1. Abrasion Modes

To understand the removal mechanisms during dielectric CMP it is interesting to compare polishing with grinding, Table 2-1.

Abrasion Mode	Mass removed via:	Scale of mass removal
Grinding	Crack propagation Fracture	Macroscopic particles μm
Ductile Grinding	Crack initiation, plastic flow, densification	Colloidal particles nm
Polishing	Bond breakage Chemical reaction	Atomic clusters Å

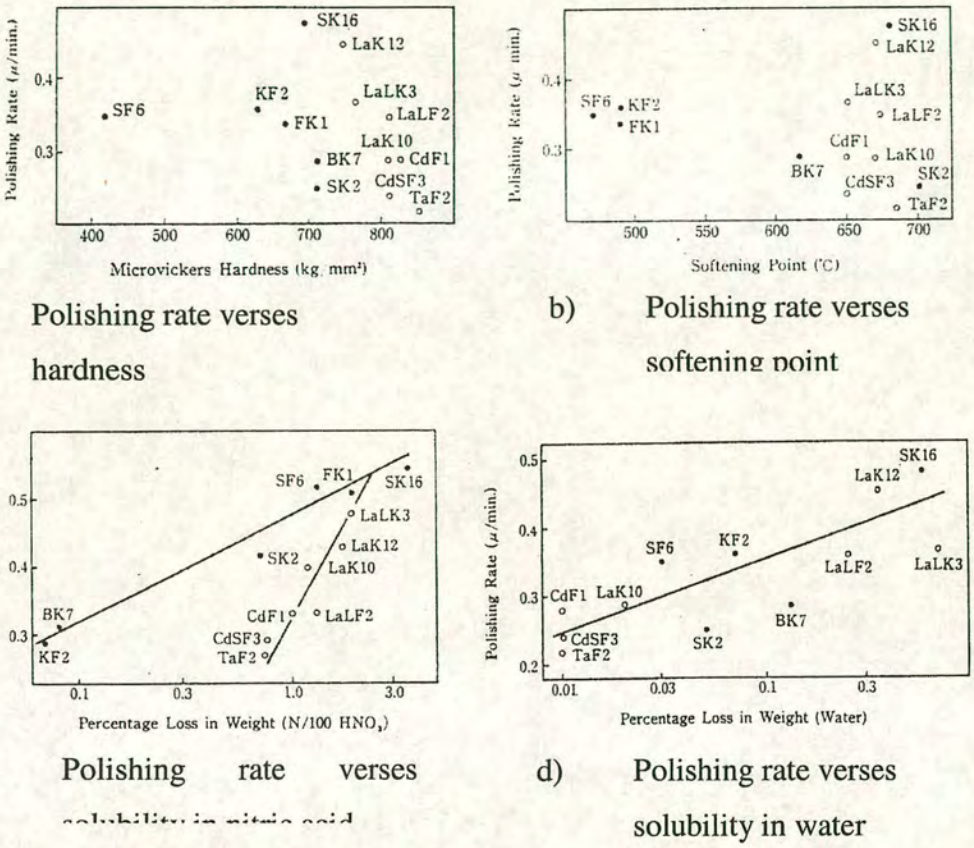
Table 2-1 Modes of abrasion[37]

The main difference between grinding and polishing is the abrasive size used, which in turn dictates the removal mode. Grinding normally employs abrasives in the order of 100μm in diameter, while in polishing the particulate size is more likely to be 10–300nm. Although larger particulate size produces a higher material removal rate it also results in a poorer final surface quality.

2.3. Removal Mechanism

Izumintani[38] compared the polishing rates of glasses with their mechanical properties and came to some surprising conclusions. He looked at polishing rate as a function of hardness, softening point, solubility in nitric acid and solubility in water, his results are shown in Figure 2.4. It can be seen that there was no correlation between removal rate and hardness or softening point, only a weak

correlation with solubility in nitric acid, but a very strong correlation for solubility in water.



a) Polishing rate verses hardness

b) Polishing rate verses softening point

c) Polishing rate verses solubility in nitric acid

d) Polishing rate verses solubility in water

Figure 2.4 Polishing rate verses hardness, softening point, solubility in nitric acid and solubility in water for various glasses[38]

This indicates, surprisingly, that polishing rate is not a function of glass hardness but is a function of its solubility in water. Hence, it turns out that using water in glass polishing is critical, as it not only performs as a coolant and transport agent but also takes an active part in the polishing process.

The question is what is the water actually doing in the glass and why is it so important? Tomozawa[39], and also Rajan[40], found that the surface of the glass is hydrated after polishing, and the depth of this hydrated layer may be as much as 20nm. This suggests that as the water penetrates the surface it may be physically modified. In a later paper Rajan[41] suggests that the penetration of the water into the surface creates material softening which allows the mechanical component to abrade material, Figure 2.5.

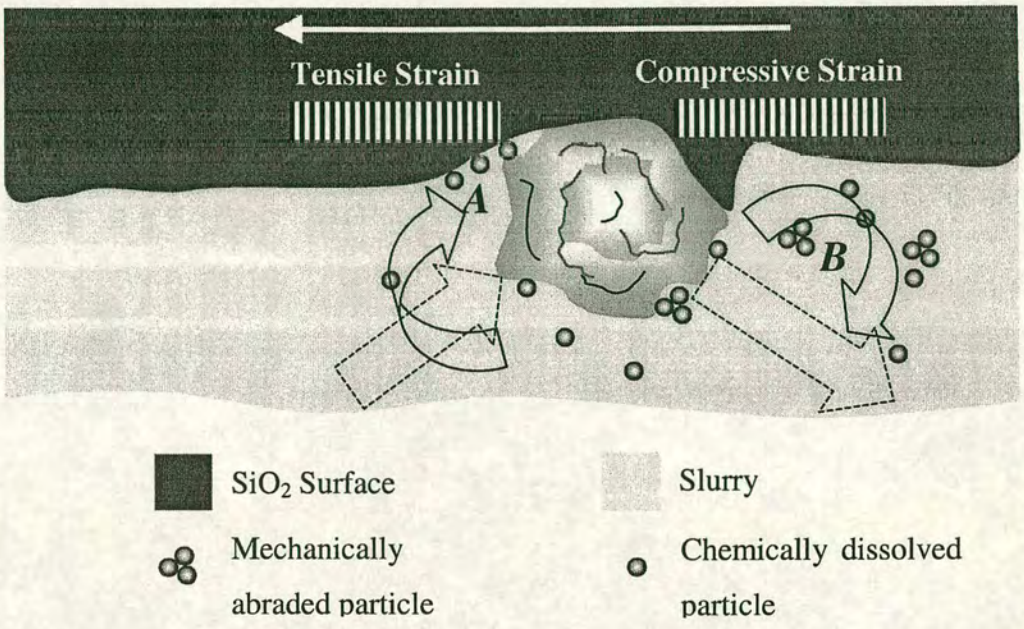


Figure 2.5 Schematic of particulate contact with oxide surface

The abrasive particulate itself is thought to play an active roll of the water absorption into the surface[42]. With it literally acting like a pump, forcing water into the surface. The actual polishing process can be broken down into specific stages:

1) Water is moved to the wafer surface by the action of the slurry
2) Water reacts with the surface augmented by the kinetic energy of the abrasive particulate as it impacts the surface
3) Some dissolution of hydrated SiO_2 by the slurry in regions of compressive strain (*B* Figure 2.5)
4) Some mechanical removal of the softened hydrated SiO_2 by impact of abrasive particle (*B* Figure 2.5)
5) Abraded and dissolved material transported away from impact site by the action of the slurry and on the surface of the abrasive particulate
6) Some re-deposition of dissolved material in regions experiencing tensile stress. (*A* Figure 2.5)

This leads to several conclusions:

1) Polishing is not merely mechanical abrasion of slurry against the wafer surface
2) The presence of water is a necessity for the removal process

Relying on chemical/mechanical action rather than abrasion avoids a mechanically damaged surface. This microscopic removal nature distinguishes it from the grinding process.

2.3.1. Polishing Mode

It is clear that the abrasive particle contacts the surface but how it is brought into contact still remains unclear. There are two possible mechanisms which may be responsible for fluid flow and wafer/pad contact (Hertzian indenter), Figure 2.6

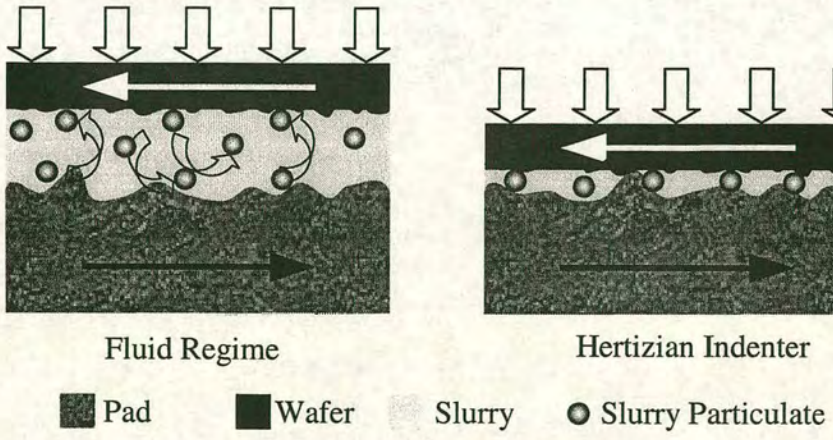


Figure 2.6 Schematic of fluid and Hertzian wear phenomenon

In fluid based erosion[43]the turbulence of the slurry, caused by the relative motion of pad and wafer, imparts kinetic energy to the abrasive particle. This energy is sufficient to cause the removal of material. In the Hertzian indenter model[44] the abrasive particle is trapped between wafer and pad and is dragged across the surface by their relative motion. In reality, however, it is thought that

the wafer/particle contact is probably caused by a combination of the two modes[45].

2.3.2. The Mechanisms of Chemical Mechanical Planarisation

In the Hertizan regime the pad is in direct contact with the wafer surface. Although the pad is ≈2mm in thickness it is only the top tens of microns that actually interact with the wafer surface, Figure 2.7.

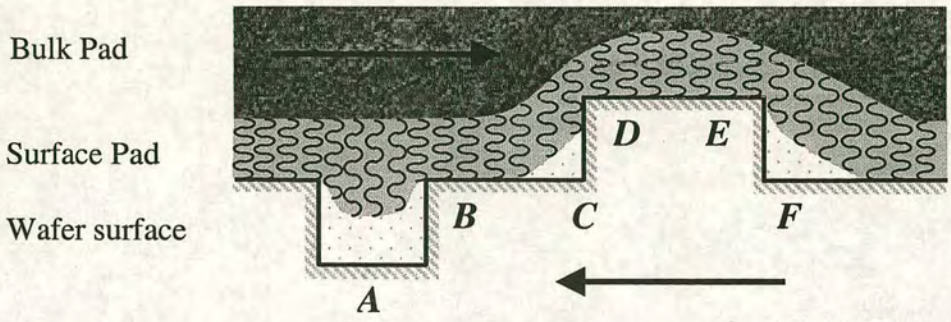


Figure 2.7 **Schematic of wafer/pad interaction, when operating in the Hertzian indenter regime**

The removal of topography depends on the enhanced removal rate at the edges of high features[46]. This is caused by the pad being forced to compress at the leading edge as it travels over the feature (*C-D* Figure 2.7). This localised pressure increase[47] causes increased material removal. The pad loses contact with the wafer surface on the trailing edge of the feature (*E-F* Figure 2.7). In the low areas between the features the pad is not deformed sufficiently to reach the bottom so no material removal occurs (*A* Figure 2.7)

Fluid based wear achieves planarisation by the fact that a velocity gradient exists in the slurry trapped between pad and wafer. Within a recess the velocity of the slurry is low while on the tops of raised features it is high. As the slurry imparts kinetic energy to the abrasive particle these too will have different velocities in the different regions. The difference in kinetic energy is sufficient to

cause a difference in material rates between the raised and recessed feature, Figure 2.8.

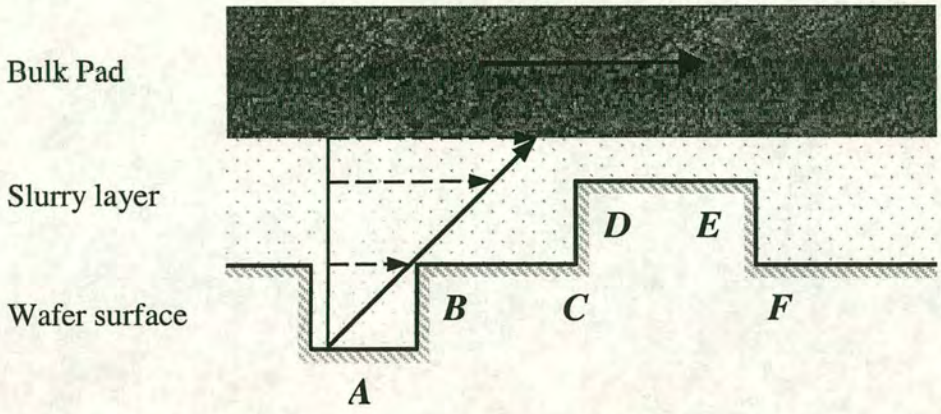


Figure 2.8 **Schematic of wafer/pad/slurry interaction, when operating in the Fluid flow regime**

2.3.3. Prestons Equation

Perhaps the best known equation in CMP is the Preston equation[48] and no writings on the subject would be complete without its mention. It is typically written as:

$$RR = P\ V\ K_P$$

Equation 2-1 **Prestons (modified) equation**
Where: RR is removal rate, P is pressure, V is velocity and K_P is Prestons Coefficient

In fact Equation 2-1never actually appears in this form anywhere in his paper, and indeed no mention of the Preston coefficient is made. It has been other authors who have coined the term which is now widely used[49]. The equation was arrived at empirically and the closest statement is:

> "Now if all the (*polishing*) blocks are equally weighted and if μ (*coefficient of friction*) is a true constant, we may state our fundamental law in a different way thus:
> The rate of polishing on a given element is proportional to the amount of felt that passes over this element per second"

Cook[36] puts this statement in to a context which is more useful in CMP:

$$\frac{\Delta H}{\Delta t} = K_p \times \frac{L}{A} \times \frac{\Delta s}{\Delta t}$$

Equation 2-2 Prestons equation after Cook[36]

Where *$\Delta H/\Delta t$ is the change in height over time t, L is load, A is area, Δs is relative travel between glass and pad and K_P is Prestons coefficient*

He goes on to state the kinetics of polishing are:

1) The rate of surface height removal is dependent on pressure, which is determined by the contact area of the surface. As polishing proceeds and contact approaches the geometrical area of the part, $\Delta H/\Delta t$ decays to some asymptotic value characteristic of the system, as does surface roughness
2) The rate of surface removal increases directly with increasing load or pad velocity

According to Equation 2-1 material removal rate is directly proportional to speed and pressure, double the speed and the removal rate will double. Some authors[50,51] found that actual removal rate did not follow Prestons equation while others[52,53] found that it did. The problem seems to lie with the Preston coefficient. It is a function of every other CMP variable apart from pressure and speed. This makes an actual real usable value almost impossible to calculate precisely. Doubling the speed of the platen may not cause an associated doubling in removal rate. The slurry flow between pad and wafer will no longer be the same, resulting in a divergence from the predicted removal rate. Higher speeds and pressures will also alter the pad temperature, due to different frictional forces, modifying the pads mechanical properties and again the removal rate.

Although the Preston equation is a good starting point to predict CMP performance it is far from perfect. As with most aspects of CMP each individual process/consumable set needs to be characterised in order to optimise CMP performance.

2.4. CMP Variables

Table 2-2 lists many (but not all) of the variables in the CMP process and their effect on process outcome. The variables in CMP can be divided into two basic types, process and consumable.

CMP Responses										CMP Factors
Removal Rate	Removal Uniformity	Planarity	Edge exclusion	Pad life	Surface finish	Defects	Selectivity	Oxide erosion	Plug dishing	
										Process Variables
										Consumable Variables
X	X	X	X			X	X	X	X	Polishing pressure
X	X	X				X	X	X	X	Table speed
X	X	X							X	Polish position on table
X	X	X		X	X				X	Slurry chemistry
	X	X	X	X					X	Slurry particle dynamics
	X	X							X	Slurry dilution
X	X	X	X				X	X	X	Temperature
X	X	X	X	X	X	X	X	X	X	Polish pad type
							X	X		Under pad type
					X			X	X	Polish pad conditioning
					X			X		Conditioning sweep
			X					X	X	Conditioning disk type
								X	X	Conditioning disk age
								X	X	Wafer back pressure
X	X		X		X		X		X	Polish time
								X	X	Wafer size
X	X	X	X	X	X	X			X	Material polished
								X		Wafer carrier
								X		Wafer backing film
								X		Carrier hole pattern
						X		X		Carrier retaining ring
								X	X	Spindle speed
								X		Carrier oscillation
								X		Wafer flatness
						X		X		Wafer extension
			X							Post CMP clean technique
X	X						X		X	Pattern density
X	X						X		X	Feature size

Table 2-2 Process and consumable variables used in CMP[54]

2.4.1. The Pad

The polishing pad, perhaps, plays the most critical role in the CMP process. It affects all aspects of polishing performance such as surface quality, planariastion ability, wafer polish uniformity and material removal rate to name but a few. Commonly used polishing pads are made out of cast or impregnated polyurethane material[59] and tend to have an open 'sponge like' texture. In addition to this the surface often has holes or grooves cut into it to aid slurry transportation under the wafer.

The mechanical properties of the pad material are extremely important in achieving uniform and repeatable results. Unfortunately these properties can be modified in a number of ways, some controllable, some not so. The pad material is sensitive to the absorption of water and to changes in temperature. Both these parameters will have an effect on the stiffness of the pad. In his paper Weidan *et al*[55] investigated the effect of temperature and water absorption of a pad on polishing performance. He found that the effect of altering the platen temperature (i.e. the bulk pad temperature) was marginal, but by altering the slurry temperature (i.e. the surface pad temperature) removal rate, and the pads' ability to remove surface features, was enhanced. He explained this by suggesting that as the pad becomes hotter it becomes softer. This allows, at the same pressure, more pad to contact the wafer thereby allowing more contact with the abrasive particles leading to an increase in removal rate. Some increase of chemical reaction may also account for the observed increase in removal rate, but no mention of this is made. The increase in planarity is a function of the softer surface asperities of the pad. When polishing closely spaced features the pad asperities can 'reach' down between them and remove material at the bottom of the trench. If that pad surface is hotter (softer) these asperities will have less mechanical strength with which to abrade the bottom of the trench resulting in a lowering of the removal rate in the low areas. Unfortunately the temperature of the small area of the pad which is in localised contact with the wafer also undergoes frictional heating[56] causing local

variations in the pad stiffness. This is probably one of the main causes of polish non-uniformity.

Pad Hardness

The most common pad in use for dielectric polishing is the Rodel IC1000. This is a composite pad comprising a (relatively) hard top pad bonded onto a softer packing pad. This overcomes a lot of the problems associated with selecting the pad hardness. If the pad is too soft it will polish the low as well as the high areas equally resulting in poor planarisation (Figure 2.9*a*). A very hard pad gives poor global uniformity because of it inability to conform to the gross wafer shape (Figure 2.9*b*). The stacked pad is used to provide good local planarity (a function of the stiffer top pad) but with the ability to conform on a wafer scale to produce uniform removal on a more global scale (a function of the softer bottom pad) (Figure 2.9*c*)

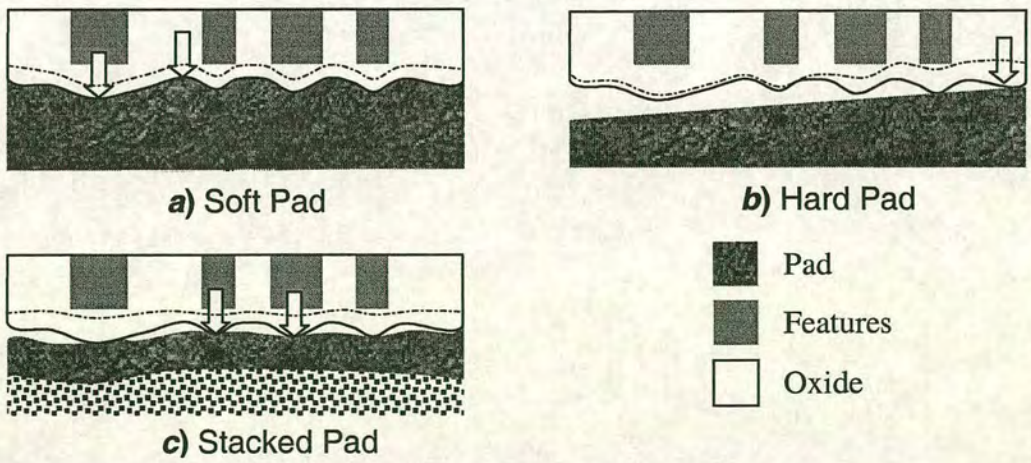
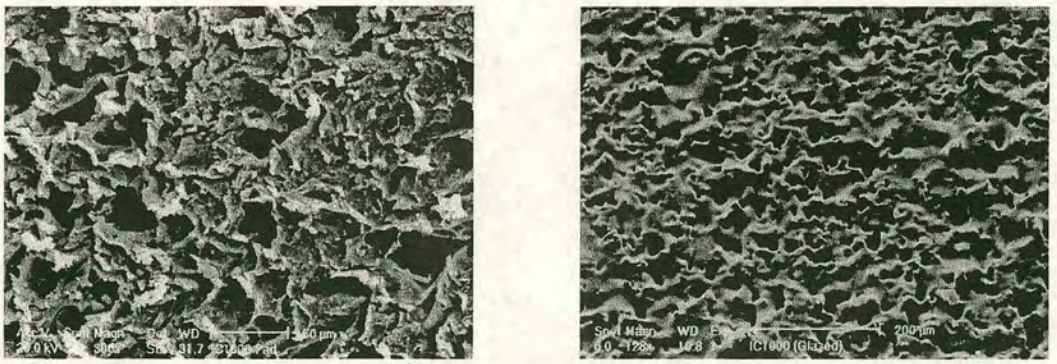


Figure 2.9 **Comparison of hard and soft polishing pads ability to deform on a wafer scale**

Pad Conditioning

Many authors have shown the importance of pad conditioning to the uniform polishing of wafers. It is common knowledge that without conditioning material

removal rate will fall[57]. This reduction in removal rate is due to a degradation of the pad surface brought about by a combination of pressure/velocity induced cold flow of the pad, which tends to smooth the surface, Figure 2.10. Caking of the pad by the abraded material and slurry results in the pad pores becoming clogged[58]. This degradation results in reduced transport of fresh slurry (slurry holding capacity of the pad) and the number of active sites with abrasive particles which take part in the removal process[59]. To restore the removal rate pad conditioning is necessary. This consists of scouring the surface with some form of roughening tool, be it a hardened steel toothed blade, stainless steel brushes or a diamond lap. The conditioning process can be carried out 'in-situ' by conditioning the pad while the wafer is being polished, or ex-situ where the pad is conditioned while the wafer is not in contact with the pad. In-situ has the advantage that polishing is continuos, and therefore has a higher throughput, but the disadvantage that the debris removed by the conditioning tool can be carried under the wafer, possible causing scratching.



a) Conditioned *b*) Glazed

Figure 2.10 SEM images of conditioned, *a*, and glazed, *b*, Rodel IC1000 polishing pad

On the Pressi E460 polishing machine conditioning is carried out using a 150mm diameter diamond annulus lap, ex-situ. As the machine is not usually used to polish large number of the same type of wafers the pad condition is not as critical as in a production environment. This is not to say that conditioning is neglected. The pad is usually conditioned for a one minute cycle between wafers, which was found sufficient that no loss in removal rate has been observed.

It is important not to over-condition the pad. Conditioning, by its very nature, removes pad material, over-conditioning therefore results in reduced pad life. Truong *et al*[60] used this fact, that conditioning removes pad material, to modify the pad profile thereby modifying the polishing rate uniformity. This study highlighted the fact that the conditioning regime can influence the final polish uniformity. As such it is as important to have a fully characterised conditioning process as it is to have a characterised polishing process.

2.4.2. Process variables

As can be seen from Table 2-2 there are many process variables to select. The effects on the polish uniformity of these variables is investigated in the next chapter. Obviously while the main objective of this work was to optimise polish uniformity, in the 'real' world the processing time would also have to be taken into consideration. So a compromise may need to be reached to achieve maximum machine throughput.

2.5. Presi Mecapol E460 CMP System

All the polishing reported in this thesis has been performed on the University's Presi Mecapol E460 polishing machine. While the polishing machine construction is not critical to the CMP result it needs to have certain key features. These are that speeds and pressure must be repeatable and that the machine is robust enough so as not to flex under load. A machine designed to be used as a research tool needs to be far more flexible in use than one designed for a production environment. The layout of the E460 can be seen in Figure 2.11 and Figure 2.12.

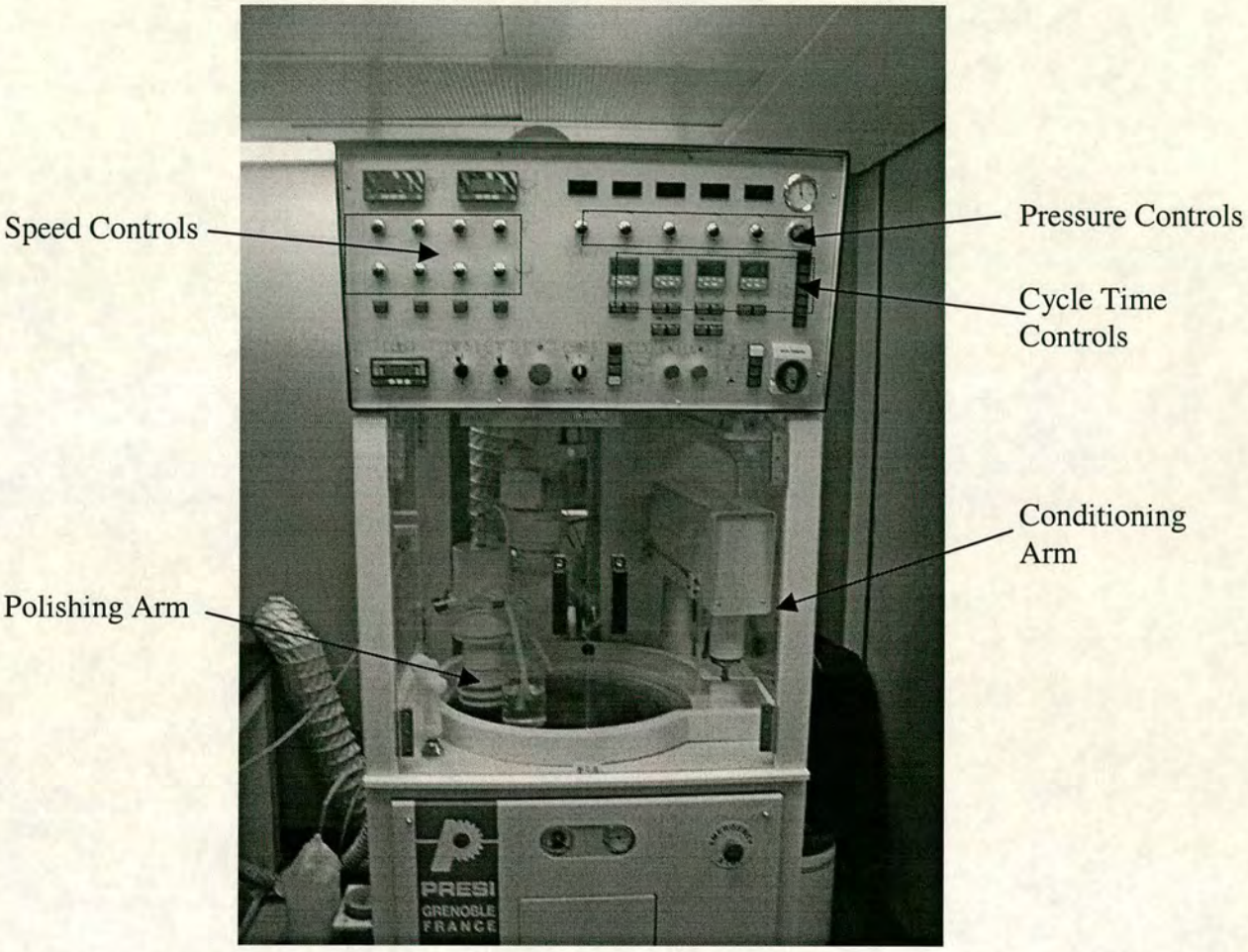


Figure 2.11 Photograph of Presi Mecapol E460 Polishing machine layout

The E460 has a 19" platen and is able to polish 75mm, 100mm, 150mm and 200mm wafers. The slurry is supplied by two separate peristaltic pumps, giving accurate control of the supply volume. It also allows the option of using two different slurries in the same cycle or in different cycles. This feature is useful if, for example, a metal polish is followed by an SiO_2 buff, as these two processes use different slurry chemistries.

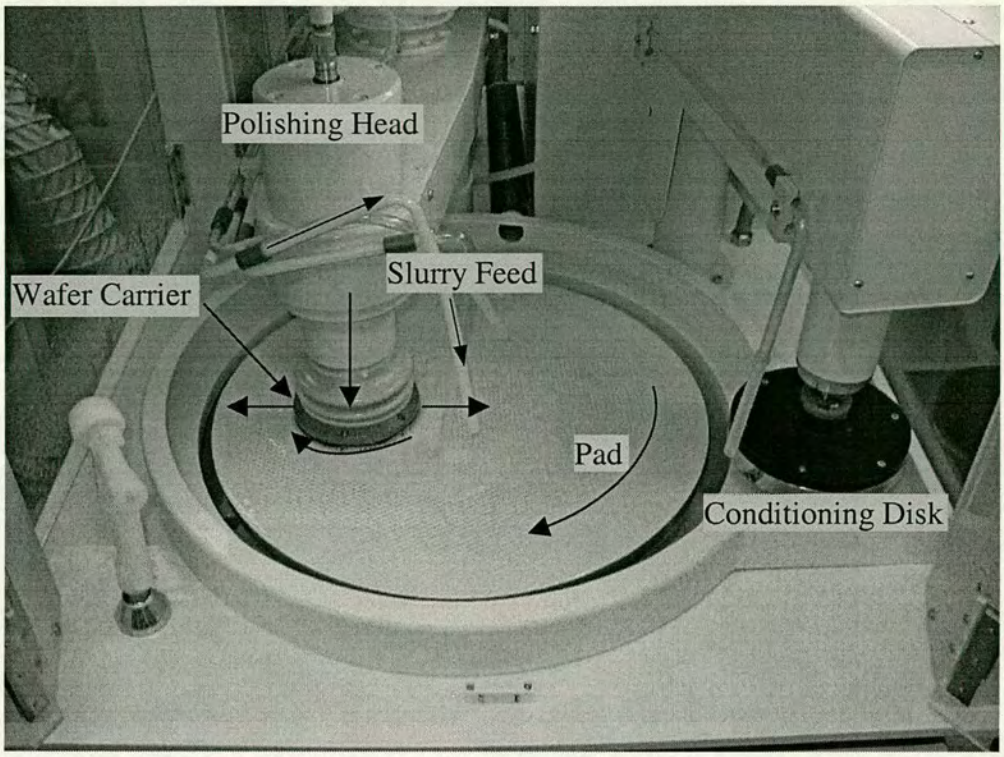


Figure 2.12 Close up of Presi Mecapol E460 Polishing machine layout

The E460 has four separate, and independently controllable, cycles:

1 Slurry spread
2 Polish with slurry 1 and/or slurry 2
3 Polish/buff with slurry 1 and/or slurry 2
4 Rinse with DI water and/or cleaning agent

For each cycle the process variables can be separately controlled; platen/head rpm, head pressure, back-pressure, cycle duration, slurry flow from two pumps. This makes the machine very flexible as all variables can be altered easily by the use of rotary controls on the front panel, Figure 2.11.

One of the greatest advantages of the E460 is the ability to quickly change platens, and hence pads, easily. This feature enables different materials e.g. SiO_2 or metal to be polished in quick succession without the need to destroy the pad for each change.

The E460 is also equipped with a water heater/chiller unit. This allows temperature controlled water to be sprayed on the underside of the platen giving the ability to control pad temperature. An in-house designed system is also in place for the control of the slurry temperature.

2.6. ECR PECVD

Much has been stated about the processes involved in material removal and planarisation ability of CMP. Another important factor is the quality of film which is to be planarised. Within the University of Edinburgh we have access to an Oxford Plasma Technology ECR PEVCD deposition system which deposits SiO_2 which is ideal for CMP.

ECR PEVCD is the ideal dielectric deposition method for dielectric films, which are subsequently subjected to CMP. It has the ability to fill small gaps and it is a 'room' temperature process. Although the deposited film is not totally stress free it induces less stress than many other deposition techniques[61].

The ECR PEVCD system consists of two chambers. The first is a microwave where the high density ECR plasma is formed. The second is downstream where the reaction occurs,Figure 2.13.

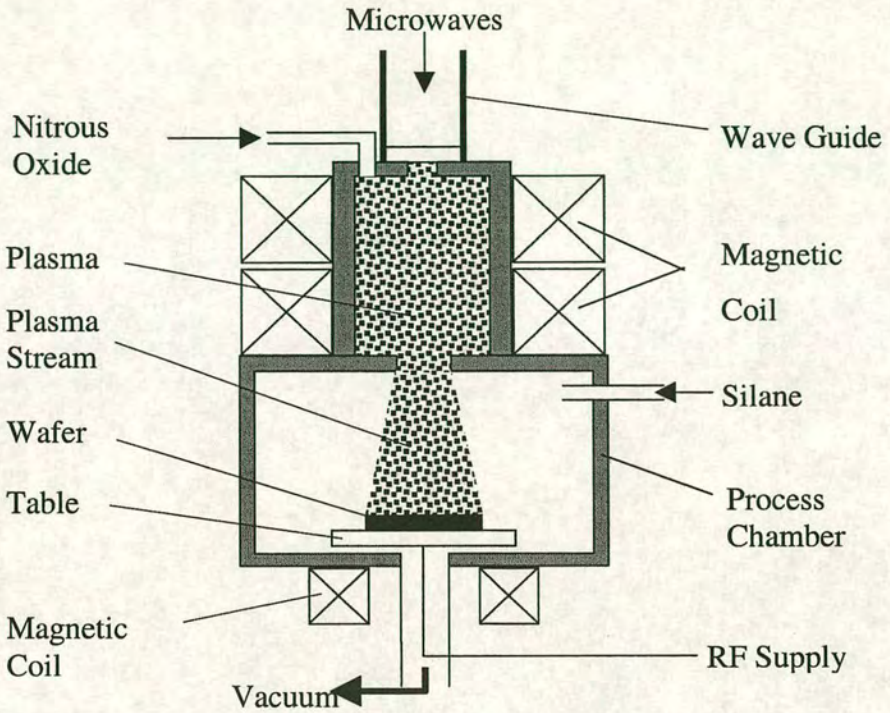


Figure 2.13 Schematic of ECR PEVCD deposition reactor

The ECR PEVCD system achieves planarisation/gap fill by its ability to etch at the same time as it deposits. By increasing the RF power it can move from a deposition process to an etch process, using a combination of both modes gap fill and local planarisation can be achieved.

Increasing the RF power accelerates the argon ions (produced in the upper chamber) and initiates a sputtering process. This sputtering process tends to remove material at the corners of features so creating facets. As the deposition process continues these facets become smaller eventually disappearing leaving the gap filled with oxide, Figure 2.14*b*.

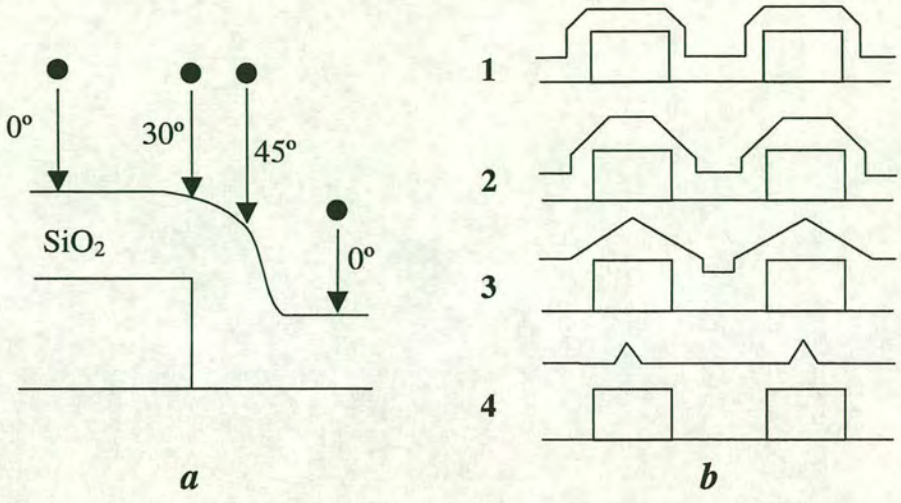


Figure 2.14 **Incidence angles of ions arriving normal to the substrate, *a*. 1, 2,3 and 4 show evolution of surface profile due to sputtering of deposited film**

The faceting effect is a function of ion incidence angle. Momentum transfer from the incident ion to the film is most favourable when the angle of incidence is 45 degrees. Consequently the sputtering rate is greatest at this angle, Figure 2.14*a*. this has the effect of the deposition rate at these areas being lower than where the ions impact at zero degrees, resulting in the gaps becoming filled and short range planarisation occurring.

The short range planarisation ability of ECR PEVCD SiO_2 also helps fill in the deep trenches which are difficult to remove by CMP alone. By increasing the RF power (or decreasing the microwave power) the ECR PEVCD deposition regime can move from one of deposition to etching[62]. Clearly if deposition is required the process must be in that regime.

The final deposited film is free of key-hole voids and other defects, providing an ideal material for CMP

3. Blanket SiO_2 CMP Optimisation

To better understand the mechanisms involved in the CMP of SiO_2 it was decided to first polish blank wafers. These are wafers with no surface topography which have been blanket deposited with SiO_2. The purpose was to investigate the effects of process and consumable set variables on polishing rate, wafer uniformity, edge effects and surface finish. All the polishing tests were performed using a Rodel IC1000 perforated pad and with Klebosol 30H50 slurry. As no other consumables were readily available it was decided that the main aim was to optimize the process variables for this consumable set.

The first tests were to determine the optimum conditions for wafer scale uniformity. The edge effect on these wafers was then investigated and methods to reduce it investigated. The sensitivity of polish uniformity to wafer back-pressure was also evaluated along with the effect of wafer bow. The surface finish of the polished surface is also important because it will influence the final optical quality of the device. AFM measurements were used to assess the effect of polishing pressure on the final surface finish.

Once familiarity with the machine and process had been gained the polishing of patterned wafers was investigated and the results of this is are detailed in the next chapter.

3.1. Blanket Uniformity Tests

The experiment was designed to evaluate a range of conditions and thereby derive the optimum ones for wafer polish uniformity. An Orthogonal matrix experiment[63] was designed which used 4 variables at 3 different levels, Table 3-1.

The 100mm test wafers were blanket coated with 2μm of thermal oxide which was used to ensure that the polish uniformity results were not influenced by any variation in deposition uniformity.

The polish uniformity was determined using a thin film gauge; with measurements being taken on a 10mm by 10mm grid with a 10mm edge exclusion zone. The standard deviation was then calculated and the results analysed.

Run #	Polishing Pressure Bar	Back Pressure Bar	Platen Speed rpm	Temperature °C
1	0.5	0.0	25	12
2	0.5	0.1	50	15
3	0.5	0.2	75	18
4	1.0	0.0	50	18
5	1.0	0.1	75	12
1'	0.5	0.0	25	12
6	1.0	0.2	25	15
7	1.5	0.0	75	15
8	1.5	0.1	25	18
9	1.5	0.2	50	12
1"	0.5	0.0	25	12

Table 3-1 Process variables used in the matrix experiments

As the different polishing conditions result in different removal rates, it was decided that all wafers would be polished until 1μm of oxide remained. To do this each wafer was polished for one minute then removed, cleaned and the film thickness measured. From the removal rate a polish time was calculated to produce a final oxide thickness of ≈1μm.

To reduce the number of variables for the matrix it was decided that both the head and platen speed would be set to the same value. The same head/platen speed was chosen because, when the wafer/pad velocities match, the average radial velocity is the same at every point of the wafer[64]. As removal rate is proportional

to velocity a uniform radial velocity should help produce uniform removal rates across the wafer.

To ensure adequate slurry supply the flow was increased at higher platen/head speeds. The criteria for the flow speed selection was that a slurry 'bow wave' must be seen in front of the wafer carrier. At higher speeds the slurry tends to be removed faster from the platen, producing a possible shortage of slurry beneath the wafer. The flow rates used were 150ml/min at 25 rpm, 200ml/min at 50 rpm and 250ml/min at 75rpm.

The pad was conditioned for 1 minute after each wafer. As the same amount of material was being removed it was not considered necessary to condition in the middle of the longer polishing cycles.

3.1.1. Uniformity Results

As can been seen from Table 3-2 and Figure 3.1 the best planarity was achieved with a head pressure of 1.5bar (Figure 3.1*b*), 0.2 back pressure (Figure 3.1*d*) and a platen speed of 25rpm (Figure 3.1*a*). The effect of temperature is not conclusive. This anomalous behavior is thought to result from the fact that the pad temperature was not measured directly. The cooling/heating water was controlled but the pad surface temperature was never monitored. As only the top tens of microns contact the wafer any modification of the pad surface temperature is likely to influence the experimental outcome. Local heating of the pad can occur through frictional heating between wafer/pad contact. Heating of the pad surface will cause it to soften, so altering its polishing characteristics. For higher speeds/pressures there will be an associated increased amount of frictional heating. This results in the surface of the pad being a different temperature than the supplied cooling/heating water. This frictional heating of the pad is thought to have produced the irregular results seen in Figure 3.1*c*.

Run #	Oxide Remaining µm	Removal Rate µm/minute	Total Polish Time Minutes	Uniformity Std. Dev. nm
1	0.964	0.0648	15.55	20.91
2	1.017	0.1167	8.55	25.53
3	0.967	0.1466	6.80	24.90
4	0.994	0.1937	5.33	31.42
5	0.952	0.2528	3.94	36.41
1′	0.970	0.0641	15.55	19.70
6	0.960	0.1098	9.08	12.38
7	0.950	0.3324	3.0	66.21
8	0.975	0.1530	6.62	13.59
9	0.980	0.2612	3.82	18.16
1″	0.974	0.0642	15.55	20.57

Table 3-2 Numerical results of the uniformity polishing tests

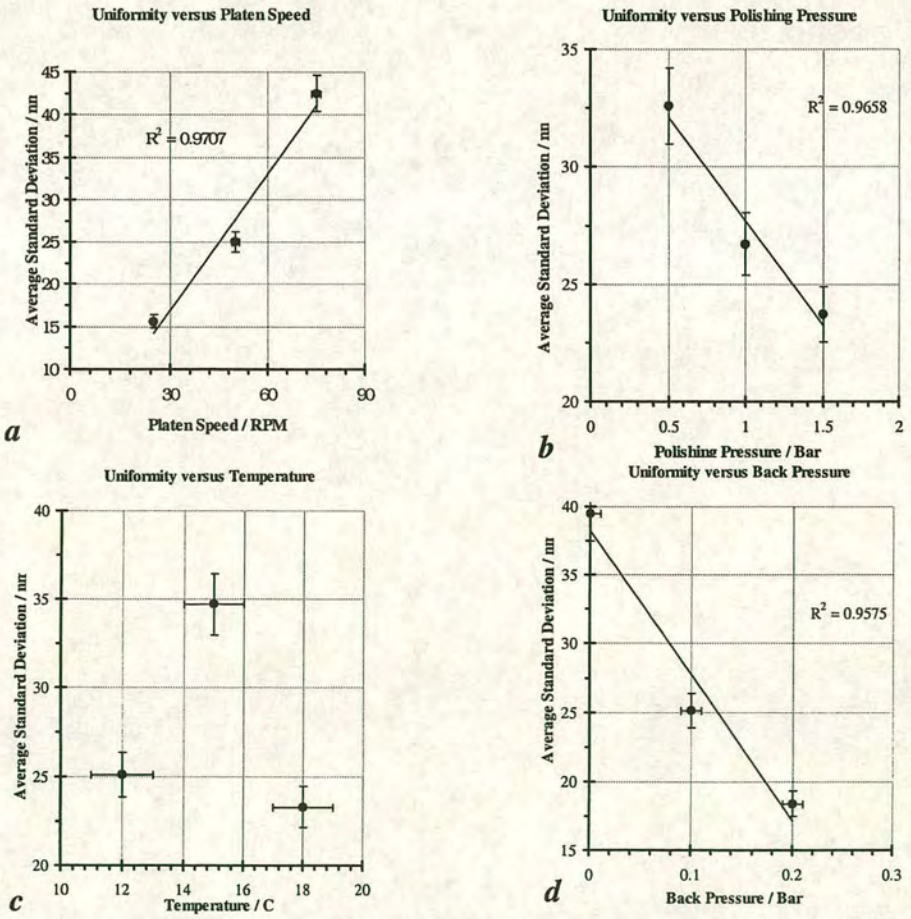


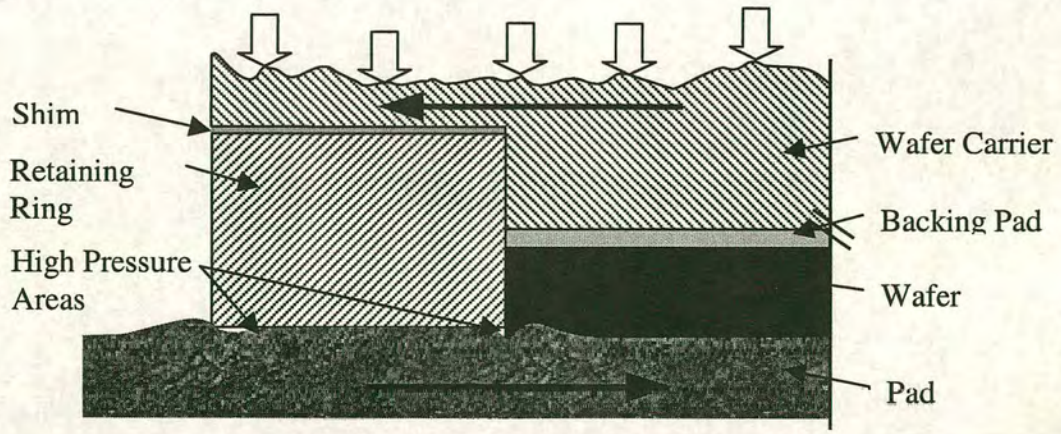
Figure 3.1 Graphical results of polish uniformity tests

As can be seen from Table 3-2 the wafers 1, 1′ and 1″ which are used to test the process repeatability, showed a 6% variation in the polish uniformity and 1% variation in removal rate. This indicates that the process is stable and repeatable.

The experiment did not include the optimum parameter combination (1.5 bar head pressure, 0.2 bar back-pressure, 25rpm head/platen speed), A wafer was polished at these settings to confirm the settings were the optimum. The resulting wafer had a uniformity standard deviation of 11.6 nm which is better than any wafer in the test.

3.2. Edge Effects

The edge effect on polished wafers is a result of pad deformation caused by the wafer traveling across it. The leading edge of the wafer causes the surface of the pad to be deformed, in much the same way as a carpet does when an object is dragged across it, Figure 3.2. This pad deformation creates localised high pressure areas causing increased polishing rates. It can be clearly visible on the polished wafers as interference fringes extending for ≈ 4mm from the wafers edge.



Note: Vertical scale greatly exaggerated

Figure 3.2 Schematic diagram of the source of the edge effect

Baker[65] modeled the effect and compared it to actual values taken from wafers polished on different pads. He came to the conclusion that the pad characteristics

play a prominent role, more so than the way that the wafer is mounted during polishing. Figure 3.3 illustrates the amount of edge effect seen in the wafers after the uniformity polish experiment previously discussed.

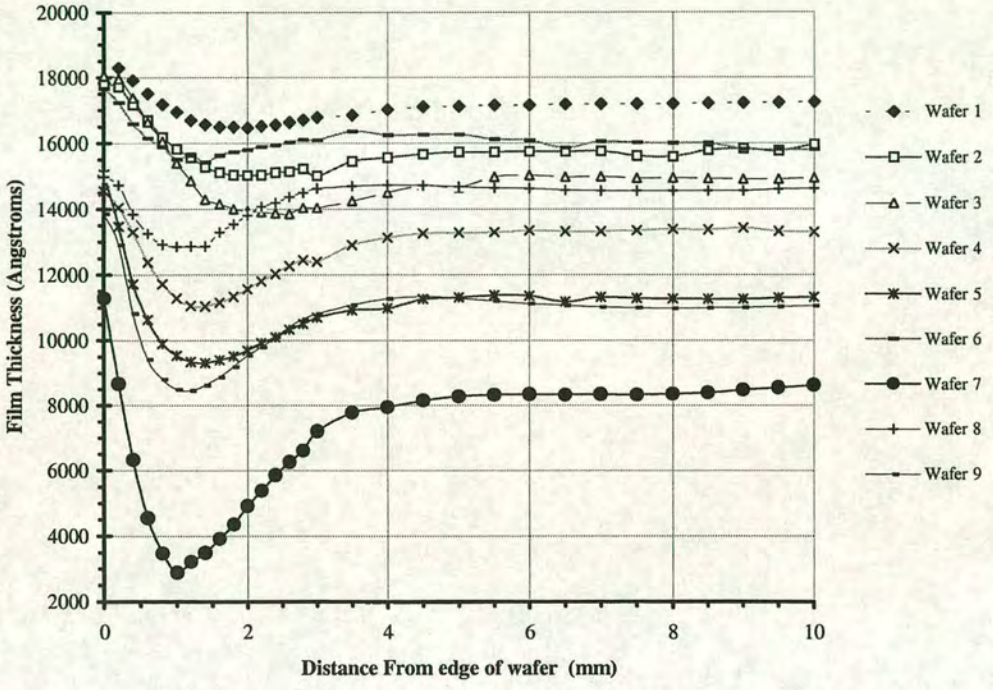


Figure 3.3 Edge effects of wafers polished in the uniformity tests

Wafer 1 exhibits the lowest amount of edge effect with a 70nm groove at 1.8mm from the edge compared with wafer 7 of 546nm at 1mm from the edge, both extend to ≈3.5mm. Wafer 1 was polished at low speed and low pressure while wafer 7 was polished at high speed and high pressure. These results support the idea that the edge effect is a result of pad deformation as more deformation would be expected at higher speeds and pressures.

The effect of adding a shim between the wafer retaining ring and the carrier, as shown in Figure 3.2, was investigated to see it the amount of edge effect could be reduced. Two wafers were polished with the same parameters, Table 3-3, one with a shim and the other without, the result are presented in Figure 3.4.

As already stated it was not feasible to investigate different pads, as once the pad has been removed from the platen it cannot be reused. Due to this all tests were performed using a Rodel IC1000 perforated pad.

Parameter	Setting
Head Speed	25 rpm
Table speed	25 rpm
Head pressure	1.5 bar
Back pressure	0.2 bar
Slurry flow	150 ml/min
Temperature	12°C

Table 3-3 Parameters used in the edge effect wafer tests

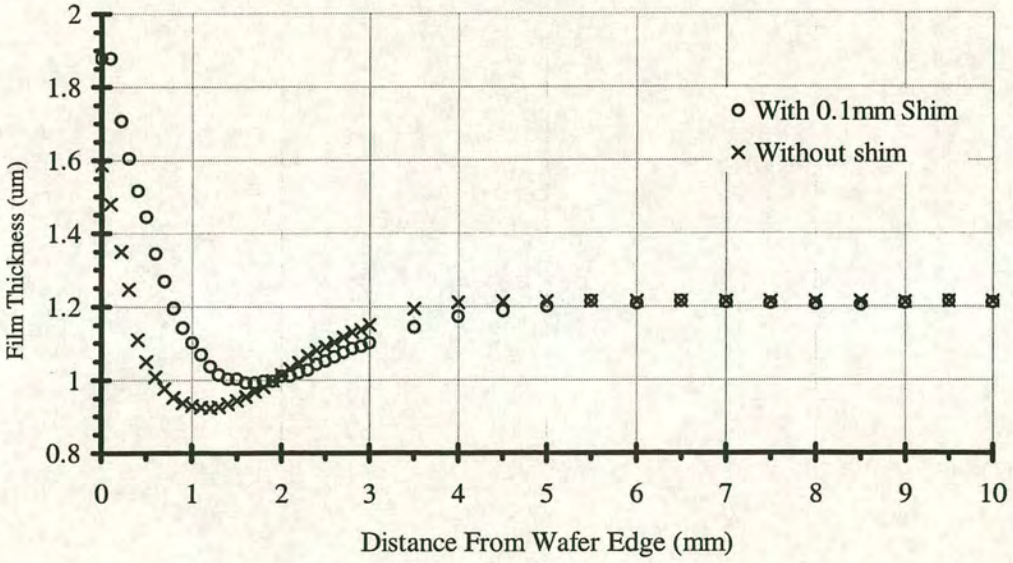


Figure 3.4 Variation on edge effect of adding a 0.1mm shim between retaining ring and carrier

The edge effect, without the shim, extends to ≈4mm into the wafer with a low point of -0.28μm (compared to the non-affected region beyond 5mm) ≈1.2mm from the edge. By inserting a shim between the wafer retaining ring and the carrier (making the wafer protrude less) the edge effect can be marginally improved. It is obvious that any die within 4mm of the edge of the wafer will suffer from a severe lack of planarity, resulting in yield loss.

3.3. Influence of Back Pressure on Uniformity

During polishing wafers tend to polish edge fast. This is caused by poor slurry transport between pad and wafer. Pad morphology plays an important role in the transportation of slurry during polishing[66,67]. Perforations or grooves are often cut into the pad surface to aid in slurry transport. Although this helps to improve wafer polish uniformity it does not remove the tendency to polish edge fast completely. Wafer back-pressure can be used to modify the polishing rate across the wafer, Figure 3.5 and Figure 3.6.

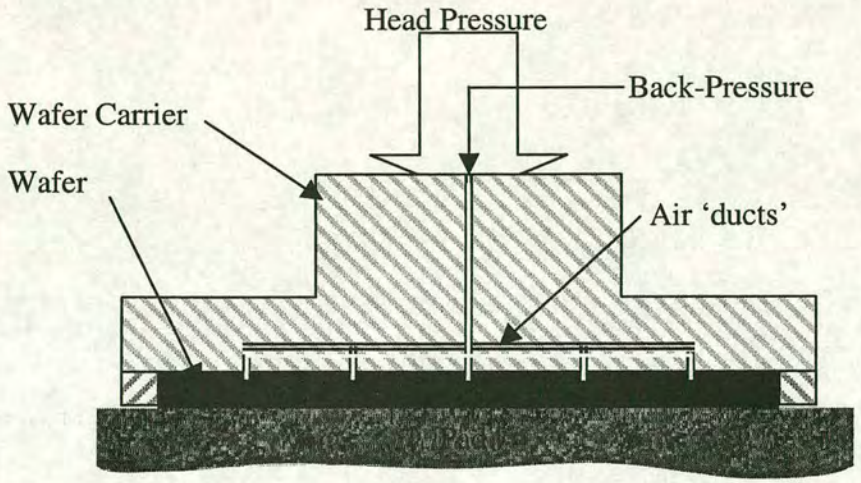


Figure 3.5 Schematic showing how back-pressure is applied to wafer

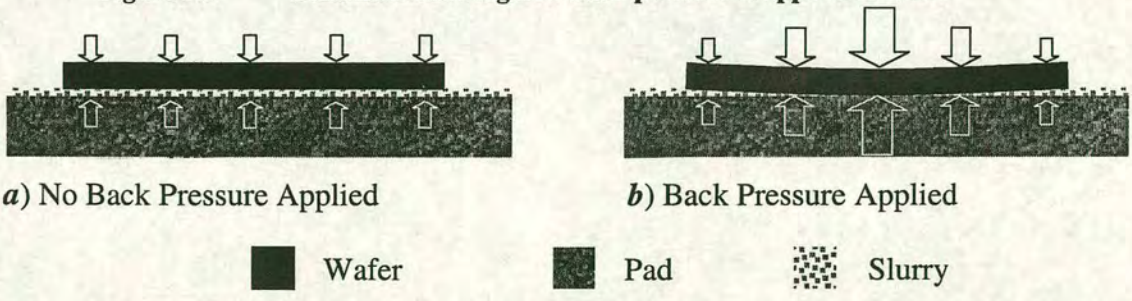


Figure 3.6 Effect of back pressure on wafer
***a*) No back-pressure, *b*) Back-pressure applied**

The application of back-pressure creates higher pressure in the center of the wafer compared with the edge. This raised pressure results in increased polishing

rates. If the correct back pressure is used this increased center polish rate can be used to counteract the natural edge fast polishing tendency[68].

Figure 3.7 shows the effect on removal rate by varying the back pressure using the process variables in Table 3-3. As the radial removal rates are symmetrical only edge to center values have been plotted. At 0 Bar back pressure the tendency to polish edge fast is seen. As the back-pressure is increased the removal rate at the center of the wafer increases faster than the removal rate at the edge. Apart from increasing the wafer center removal rate increasing the back pressure also increases the global removal rate because, although the back pressure is localised, it still acts on the whole wafer surface.

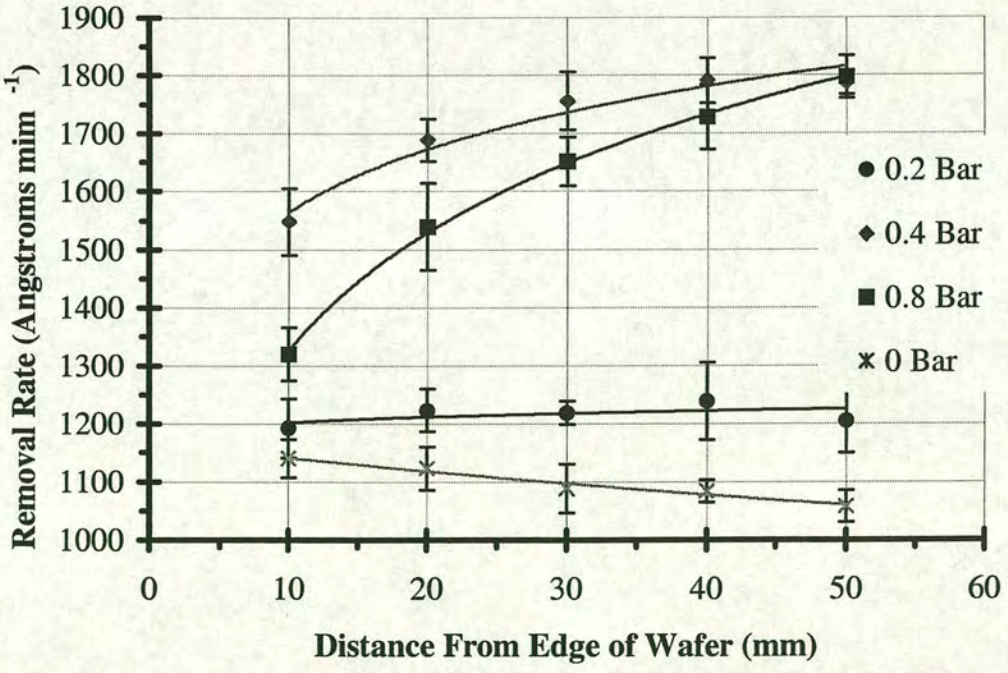


Figure 3.7 The effect of back pressure on oxide polish rate on 100mm wafers

Increasing the back-pressure from 0.6 Bar to 0.8 Bar produces an anomalous result. It appears that although the center to edge removal rates are less uniform there has been an overall reduction in removal rate. This is a result of poor slurry

transport under the wafer. As the back-pressure is so high air travels between the wafer and backing pad and escapes around the periphery of the wafer. This manifests itself as bubbles in the slurry 'bow wave' in front of the wafer carrier. These bubbles have the effect of prohibiting the slurry from being transported under the wafer, leading to an overall lowering in the polishing rate.

3.3.1. Use of Back Pressure to Reduce Deposited Film Non-Uniformity

The use of back-pressure makes it possible to establish a uniform removal rate across the wafer. This results in a uniform film thickness, which is necessary for further processing requirements. For example, via cutting, if the film is of different thickness it will result in some vias being over etched while some maybe under etched.

Using settings which give uniform removal rate is necessary if the pre-polished film is of uniform thickness. The ECR PEVCD machine used in this work tends to deposit a center thick film. If this film was polished using a process with a uniform removal rate across the wafer the resulting film thickness will also be center thick. By appropriate use of back-pressure it is possible to 'over polish' the center to create a uniform final film thickness, Figure 3.8.

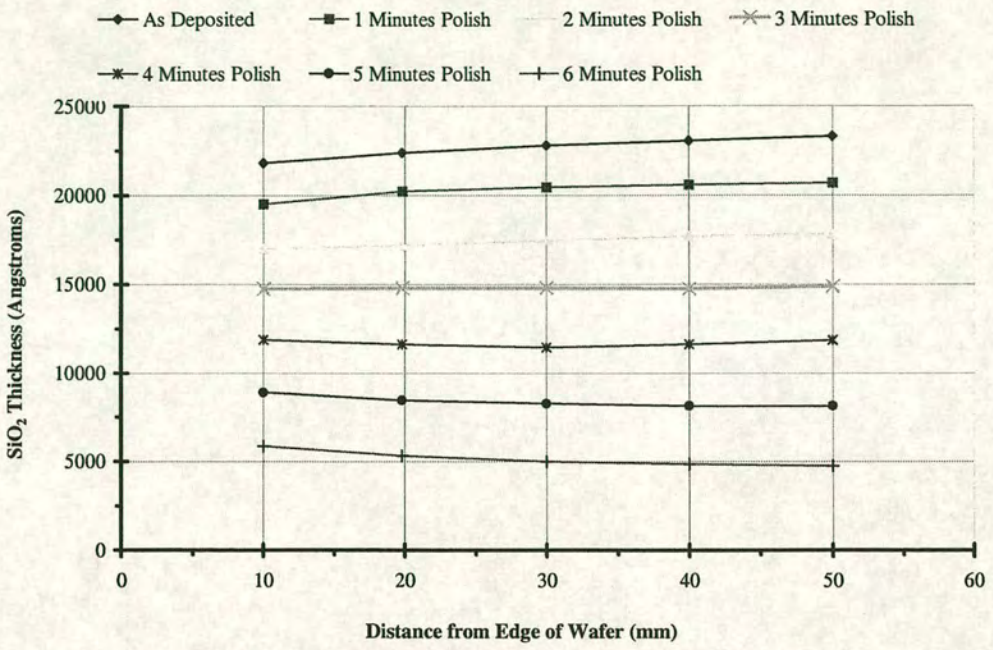


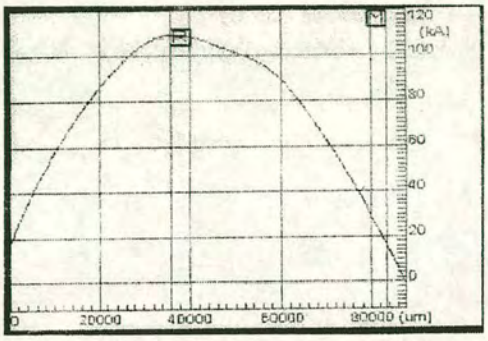
Figure 3.8 Effect of back-pressure on film uniformity

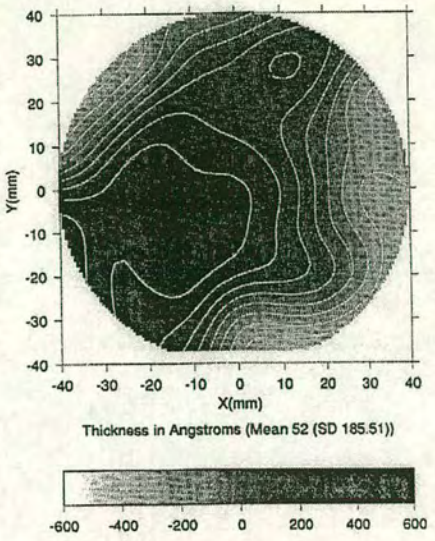
A polishing time of 3 minutes produces a uniform film thickness. After this time the back pressure could be adjusted to produce a uniform removal rate across the wafer. Alternatively the back pressure could be set to produce a uniform film thickness at the correct thickness in one step.

3.4. Effect of Wafer Bow

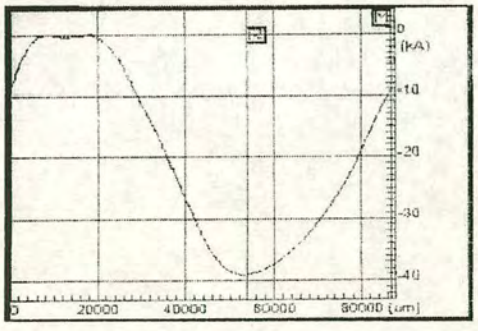
It has been suggested by Zhang[69] *et al* that the shape of the wafer may influence the polishing uniformity. To investigate this three 100mm wafers were selected which had a large amount of warp, Figure 3.9. The wafers were polished with the same process variables used in the edge effects tests, Table 3-3.

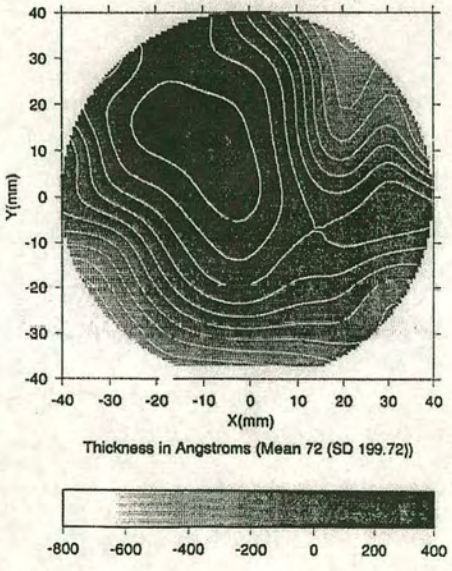
a) Surface profile showing wafer warp and final film uniformity



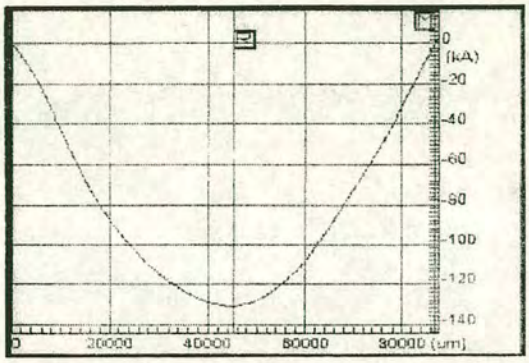


b) Surface profile showing wafer warp and final film uniformity





b) Surface profile showing wafer warp and final film uniformity



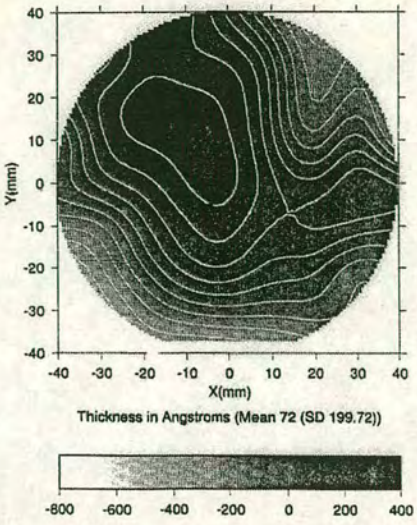


Figure 3.9 Surface profiles and surface uniformity plots of the 3 wafers used in the wafer bow tests

It can be seen that although the wafers were warped by as much as ±14μm no significant difference in polishing uniformity can be seen. It is thought that the reason for this is that the polishing head pressure, 2 Bar, is far greater than the force necessary to flatten the wafers. So although there must be a pressure difference caused by the wafer warp it is negligible when compared to the head pressure used while polishing. If, however, a lower head pressure was used the wafer bow induced pressure may play a more prominent role.

3.5. Post-CMP SiO_2 Surface Finish

The quality of the polished oxide surface is important because it affects the final mirror quality. To investigate the surface roughness two wafers were polished and then examined by AFM. The process variables of the wafers can be seen in Table 3-4, with both being identical except for the head pressure and polish times.

Parameter	Wafer 1	Wafer 2
Head Speed	25rpm	25rpm
Table speed	25rpm	25rpm
Head pressure	2bar	0.5bar
Back pressure	0.2bar	0.2bar
Slurry flow	150ml/min	150ml/min
Temperature	12°C	12°C
Polish time	2 minutes	4 minutes

Table 3-4 Process variables used in surface finish tests for wafers #1 and #2

Two scan sizes were used to obtain the roughness value, 1μm x 1μm and 10μm x 10μm. The 10μm x 10μm AFM images can be seen in, Figure 3.10, wafer 1 and Figure 3.11, wafer 2., with the tabulated results presented in Table 3-5.

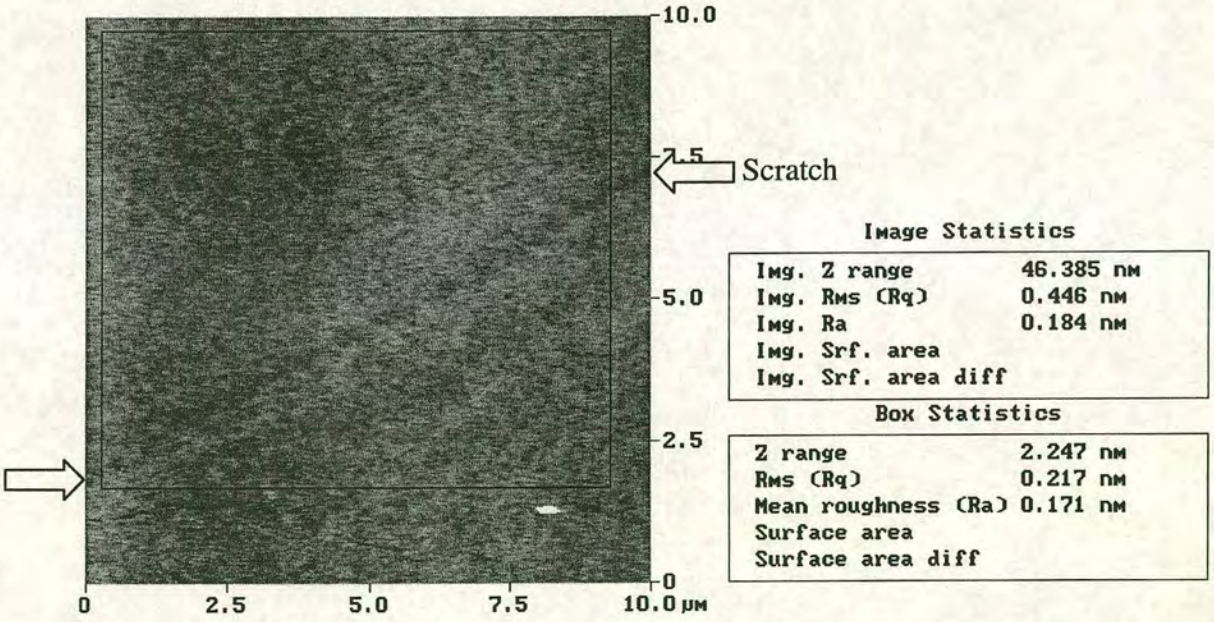


Figure 3.10 AFM of typical surface finish test wafer 1 (2 bar head pressure)

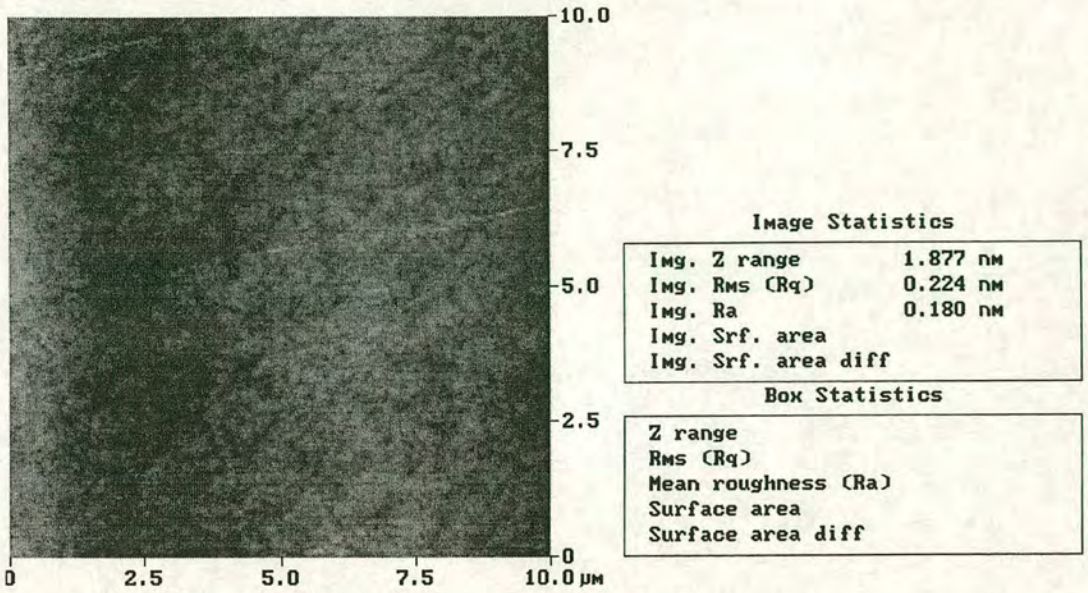


Figure 3.11 **AFM of typical surface finish test wafer 2 (0.5 bar head pressure)**

Wafer #	Scan Size	RMS
1 (2 Bar)	1μm x 1μm	0.20nm
	10μm x 10μm	0.21nm
2 (0.5bar)	1μm x 1μm	0.18nm
	10μm x 10μm	0.22nm

Table 3-5 **Surface finish of polished wafers #1 and #2**

It can be seen that both surface finishes have sub-nanometer roughness values, with little difference between them. If Figure 3.10 is examined closely a 'large' scratch can be seen running across the surface (between the two arrows). This would indicate that the wafer has been in contact with the pad which supports the idea of polishing in the Hertzian indenter regime. The lack of any large surface scratches in Figure 3.11 indicates a more fluid type polishing regime. This would be expected as wafer 1 was polished at four times the head pressure of wafer 2, although what is a surprise is the similarities in the surfaces roughness. This would indicate a large process window exists, and that the quality of the surface is not acutely sensitive to process parameters.

3.6. Conclusion and Comments

It has been shown that a polish uniformity of better than 12nm standard deviation can be achieved on a 100mm wafer. A sub-nanometer RMS surface finish is also achieved using the same polishing parameters.

The wafer edge effect appears to be a function of process variables, particularly head pressure and platen speed, and not wafer mounting. The largest edge effects were seen to occur on wafers polished at higher pressures and high speeds. Although different in depth all wafers exhibit an edge effect which extended by ≈3.5mm from the edge of the wafer.

Wafer warp does not seem to affect the polish uniformity although it is thought that this is due to the high head pressure. The use of lower head pressure may produce problems with polish uniformity.

Back-pressure may be used to remove non uniformity in the deposited film thickness, although this is limited to radially symmetric non-uniformity.

4. Patterned Oxide CMP

The polishing of blanket deposited oxide is a relatively easy task. The polishing of patterned wafers is a far more difficult proposition. As the aim of this study was to investigate methods to planarise real devices this chapter focuses on the polishing of patterned wafers. All work carried out in this chapter is aimed to achieve the planarisation of the 512^2 device. The main objective is to produce a smooth flat surface upon which high quality mirrors can be deposited. The use of any metal polish steps, either mirror damascene or via damascene, also requires that the surface is flat and free from any surface topography.

The biggest problem encountered when polishing this type of device is that the drive circuitry creates a feature dense region surround by a featureless region. This mesa is in the order of 1.6μm above the surrounding field area, seen in Figure 4.1.

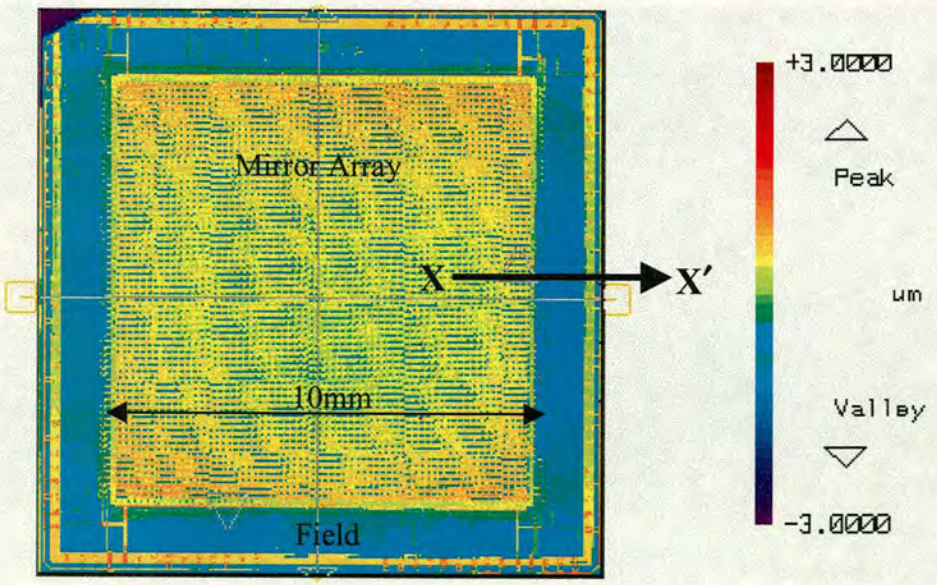


Figure 4.1 **White light interferogram of the 512^2 device as received from the foundry showing array step height and the central feature dense area.**

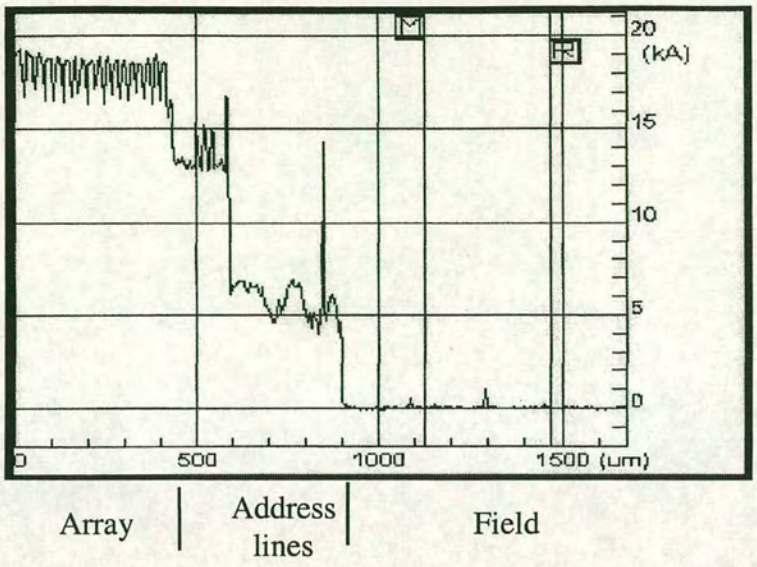


Figure 4.2 Surface profile trace along XX′ showing array step height

Difficulties arise when polishing large arrays of small features. CMP is very sensitive to variation in feature density. It polishes single, isolated features, at a higher rate than groups of features the same size, Figure 4.3. Isolated features are planarised quickly but features which are spaced closely together are removed more slowly[70].

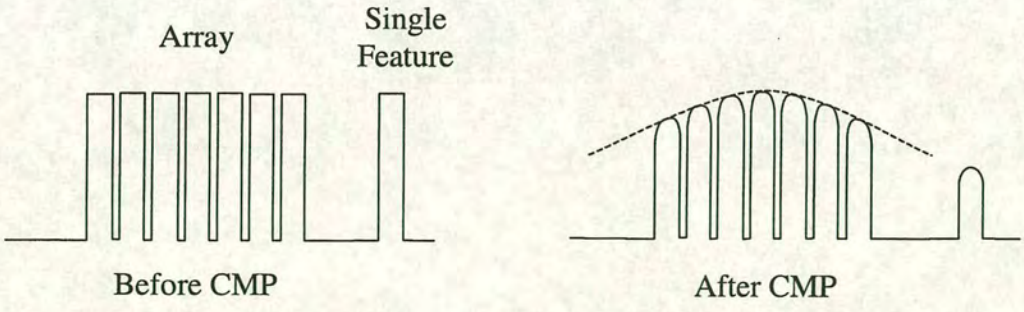


Figure 4.3 Schematic of feature dense area pre and post-CMP

This creates a non-uniform removal rate across the feature dense area. Features in the middle of the array are polished more slowly, than those at the edge, creating a 'rounding effect'. This is a result of the pads' inability to deform into the spaces between the features and the natural removal mechanism of raised features. The removal of surface topography depends on the increased pad

pressure at the edges of the features. This pressure profile results in the edges being removed before polishing starts at the center. The feature thus exhibits a rounded profile. When feature dense areas are polished the same single feature rounded profile is seen superimposed on the entire dense feature region.

Another area of importance is the surface quality of the oxide post-CMP, although if the devices are to undergo a further metal CMP step this may not be so critical. The surface finish must be of sufficient quality (low roughness) to allow highly specular aluminum to be deposited. Post CMP cleaning must be very thorough, not only do the abrasive particles left behind cause reliability concerns they also degrade the quality of the sputtered aluminum, causing a deterioration in the optical quality of the mirrors.

The following chapter describes the source of this problem and its cure using a post-CMP etch to reduce the array step height before polishing.

4.1. Experimental Details

As the cost of fully processed foundry wafers made it impractical to develop a polishing methodology using actual devices a test pattern needed to be devised. The existing 512^2 mirror mask, shown in Figure 4.4, was etched into ≈1.6 μm of aluminum, which had been sputtered coated onto 100mm diameter wafers.

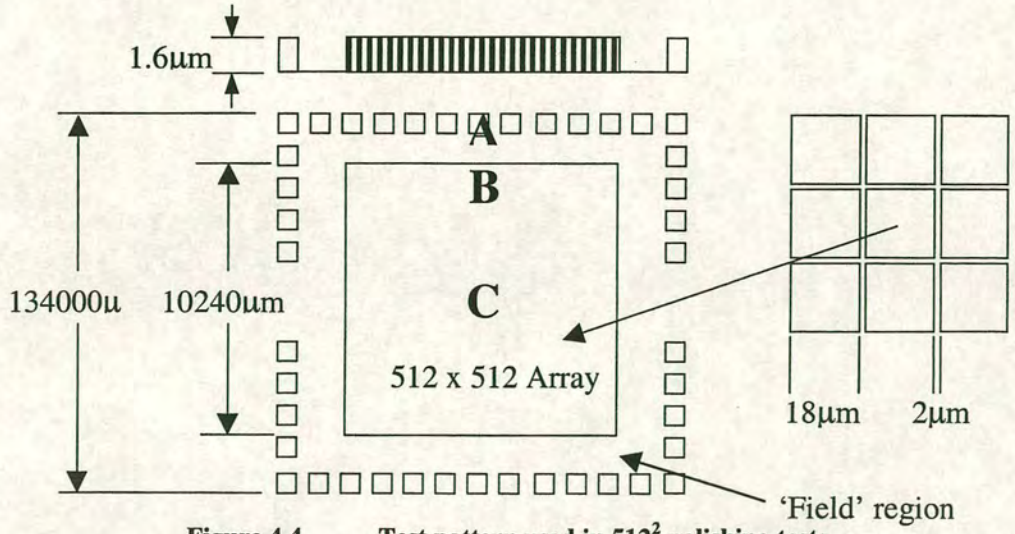


Figure 4.4 Test pattern used in 512^2 polishing tests

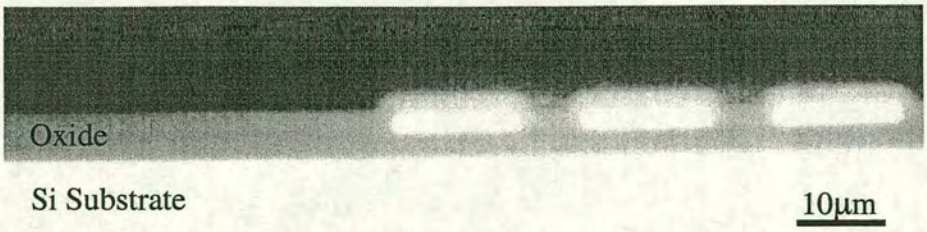


Figure 4.5 Photomicrograph of cross section of edge of test pattern before CMP

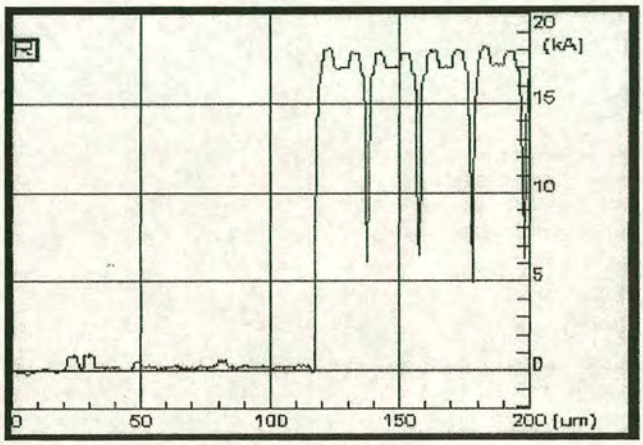


Figure 4.6 Surface profile trace of edge of test array before CMP

As the mirror mask has 18μm mirrors the final feature density produced, (85%) would have been higher than that of the real device of (50%), which would alter the polishing characteristics. To overcome this wet etching was used to define the test pattern. The use of wet etching made it possible to over-etch the pattern to produce 15μm square pixels. This made the final array feature density, 56%, more closely matching that of the real device. After resist removal 3μm of ECR PECVD SiO_2 was deposited, Figure 4.5 and Figure 4.6.

4.2. Planarity Evaluation

The measurement of the polishing uniformity proved difficult to evaluate. Initially a surface profiler was used to measure the post–CMP profile over the array, but this was found to have several drawbacks. As the die is relatively large, >10mm, an equally large scan length was needed. The vertical height scale is in

the order of nanometers whereas the horizontal distance is millimeters. As the wafer itself is not flat the amount of bow in a trace can be as much as 10μm. A typical post-polish surface profile can be seen in Figure 4.7

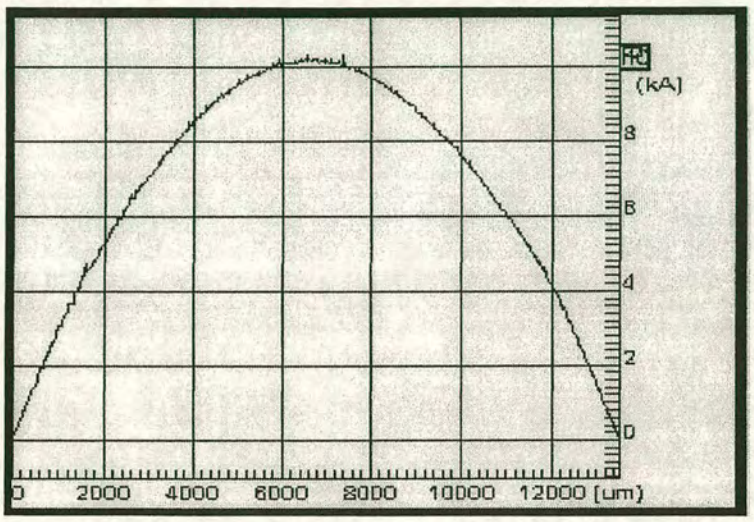


Figure 4.7 Surface profile of polished die showing wafer warp swamping out the trace

Any information regarding the planarity of the array is swamped by the large amount of die warp.

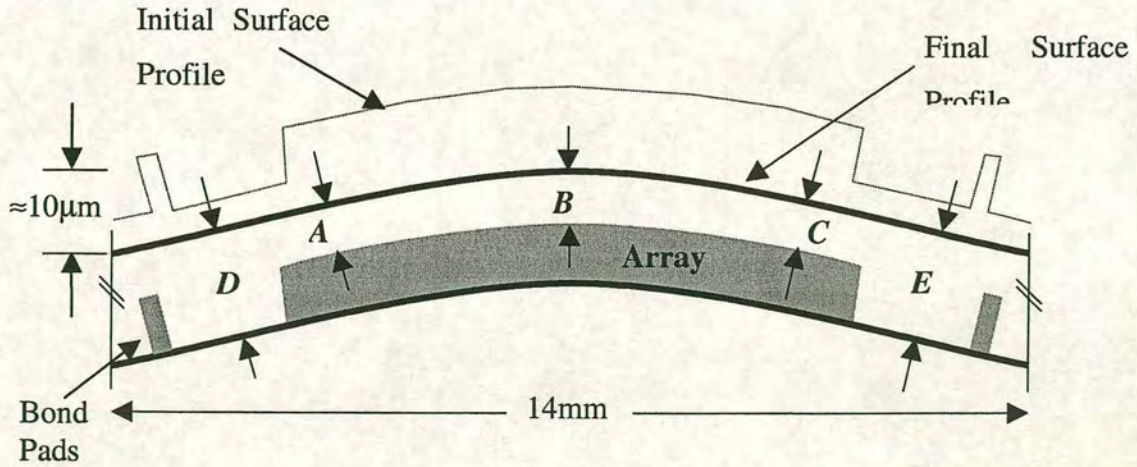


Figure 4.8 Schematic explanation of surface profile trace in Figure 4.7

This highlights an important limitation of the polishing process. It produces 'smooth' and not flat surfaces. It can remove all the surface topography on a

device but it cannot produce a 'flat' device. During polishing the wafer is forced against the pad by the application of the head pressure. This results in the wafer being flat, apart from a slight back-pressure induced curvature, during polishing. On release of the pressure the wafer returns to its original shape, i.e. bowed. Therefore CMP cannot remove wafer warp, either inherent in the wafer itself or induced by the circuitry deposited on it. The measure of the success of the polishing process must be its ability to achieve a smooth, feature free surface. The criteria in this work was to achieve a uniform oxide layer remaining over the array area after the polishing process, Figure 4.8. Locations *A*, *B* and *C* must have the same oxide thickness At positions *D* and *E* the oxide thickness minus the array step height should also be equal to *A*, *B*, and *C*. This would then produce an oxide surface which is parallel to the underlying wafer. If this is achieved the polishing process has been optimised and no further improvements can be made.

The effect of wafer warp on the performance of microdisplays is much more problematic than it is for standard ICs and will discussed in Chapter 10.

A more useful assessment of the polishing performance is therefore to directly measure the oxide remaining over the array. This was done using an optical thin film gauge. The disadvantage of this method was that is took approximately 3 hours to measure each site and a further 1 hour to plot the acquired data. It was for this reason that visual inspection of the interference fringes over the array area were used as initial indicators of polishing performance. Only wafers which exhibited good fringe patterns (few fringes) across the array were measured.

4.3. Test Pattern Polishing

Initial tests used the same parameters that gave the best wafer scale uniformity, i.e. slow speed/high pressure. On visual inspection they were found to contain a great number of interference fringes indicating a non-uniform oxide thickness over the array area. It is known that the stiffness of the pad has a speed dependency[71], which results in an effective increase in pad stiffness as the platen

speed increases. This relationship was investigated by increasing the platen speed in 10rpm intervals and observing the resultant fringe patterns within the array. The best, i.e. fewest fringes, were seen at high platen speeds supporting the proposition that a pads stiffness will increase, and thus remove surface features better at higher speeds. Although high speeds reduced the number of fringes it did not remove them completely. The best uniformity i.e. least number of fringes, were obtained by using the process variables stated in Table 4-1

With the platen speed now at 60rpm it was found that to maintain a slurry 'bow wave' in front of the wafer the slurry flow also needed to be increased.

Parameter	Setting
Head Speed	60 rpm
Table speed	60 rpm
Head pressure	1.5 bar
Back pressure	0.2 bar
Slurry flow	250 ml/min
Temperature	12°C
Pad	Rodel IC1000
Slurry	Klebosol 30H50

Table 4-1 Polishing parameters used in the initial pattern polishing tests.

To accurately assess the amount of polish non-uniformity one die was selected and measured using the thin film gauge, the results can be seen in Figure 4.9.

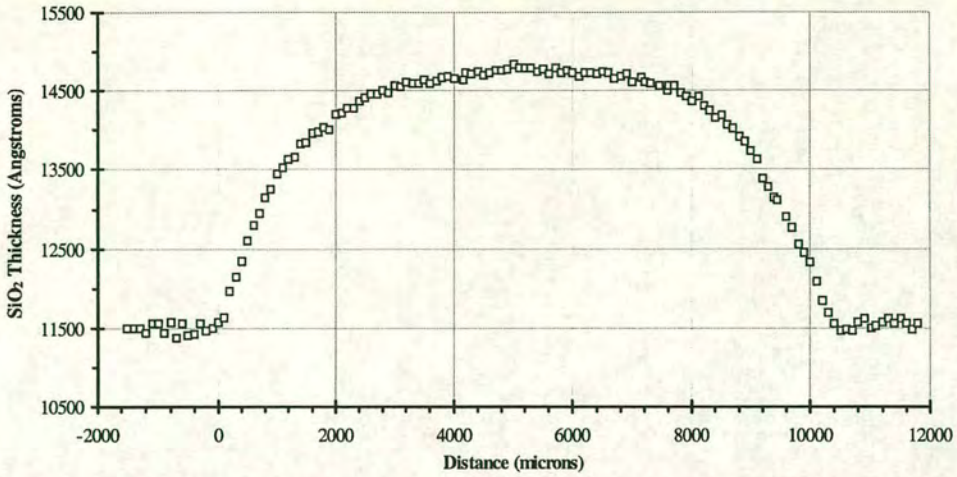


Figure 4.9 **Profile of oxide over test pattern after polishing with Table 4-1 (The array is between 0 and 10000μm)**

The profile of the array mesa now exhibits a 'domed' shape. It must be remembered that this is a line representation of a three-dimensional shape although as the array has 'square symmetry' the amount of 'doming' will also be symmetrical The array center is ≈0.3μm higher than the surrounding area. To investigate if this profile would change over time the wafer was polished and measured at 1 minute intervals until it had been polished for a total of 21 minutes, Figure 4.10.

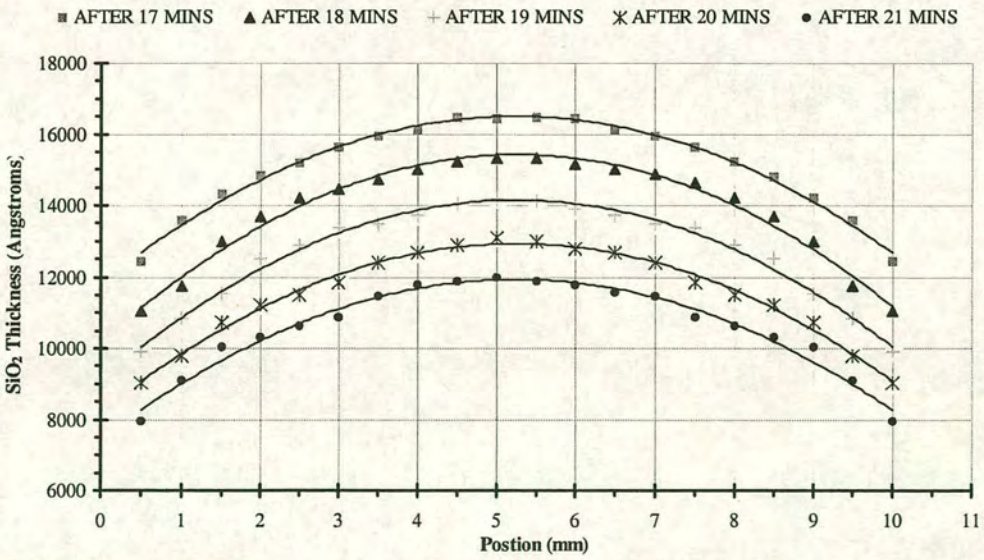


Figure 4.10 **Time evolution of polished array profile**

From this it can be observed that the oxide thickness profile over the array, once established, does not alter with time. Further polishing merely reduces the thickness and does not alter the profile. This indicates that the removal rate is constant across the mesa region. To further confirm this the oxide thickness remaining at the edge and the center of the array, (positions *B* and *C*, Figure 4.4) along with an outlying bondpad (position *A* Figure 4.4), are plotted in Figure 4.11 as a function of polishing time.

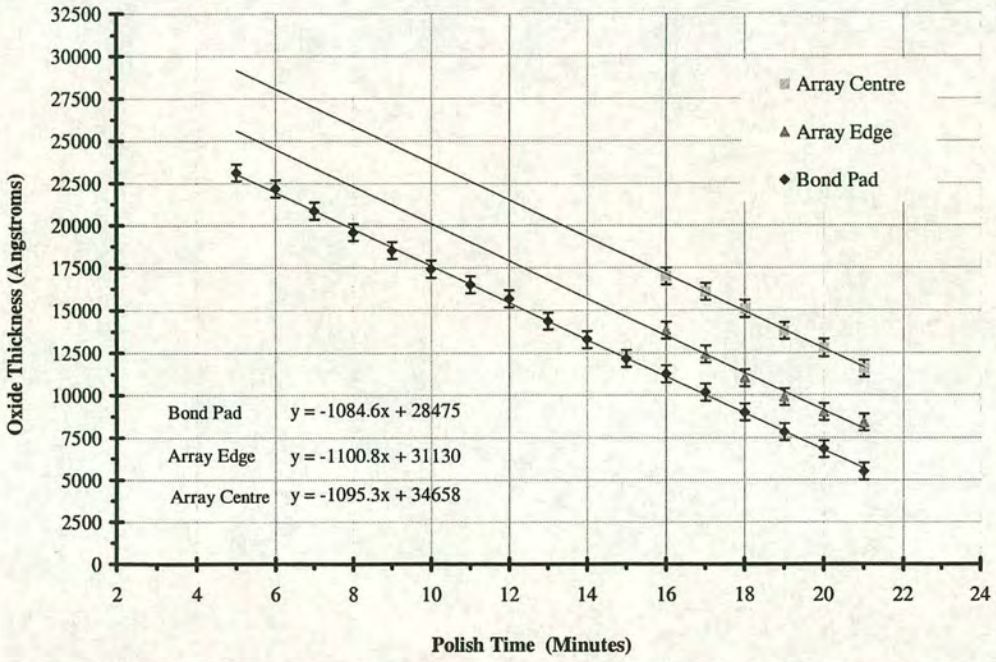


Figure 4.11 Oxide thickness for array edge and center and bondpad

The oxide thickness over the array could only be measured after 16 minutes of polishing. This is because the thin film gauges' sample area is 40μm in diameter and the 'mirrors' within the array are ≈15μm square. It is possible to reduce the spot size by increasing the objective magnification. Unfortunately this results in a loss of measurement range. At 100 times magnification the spot size is 10μm and the measurement range is between ≈1.8μm to ≈0.6μm. The oxide over the bond pad can be measured using the 10 times objective because it is 120μm square.

It is apparent from the gradients of the points in Figure 4.11 that the three polishing rates are identical and thus the array dome will not be removed using this process variable set.

It was seen that the features within the array were removed, to within 80% of their initial height, within the first 4 minutes of polishing. After 10 minutes no structure could be seen on the array surface

4.4. Pre-CMP Oxide Etch Back

To overcome the problem of array domeing a pre-CMP oxide etch was developed. 3μm of ECR PECVD oxide was deposited over the aluminum test pattern then covered with photoresist and patterned to leave the array mesa exposed. Reactive Ion Etching (RIE) is then used to reduce the mesa step height.

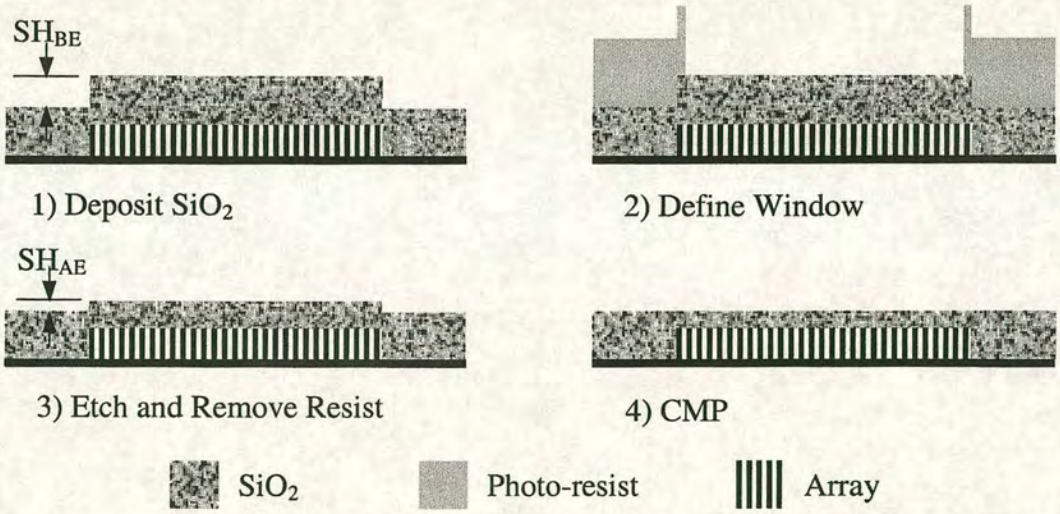


Figure 4.12 Schematic of pre-CMP etch back method

The etch-back reduces the height of the low frequency (large) features, in this case the array mesa, which is the most difficult to remove by CMP. The smaller surface features, within the array, are left largely unaffected by the etching process. The final array therefore has the same feature density as the original but with a reduced step height.

The final step height, SH_{AE} was found to be critical. The first test was to etch back to a zero SH_{AE} which left a level surface before CMP. The wafer was then polished for 10 minuets with the process conditions in Table 4-1. The result of the CMP process can be seen in Figure 4.13

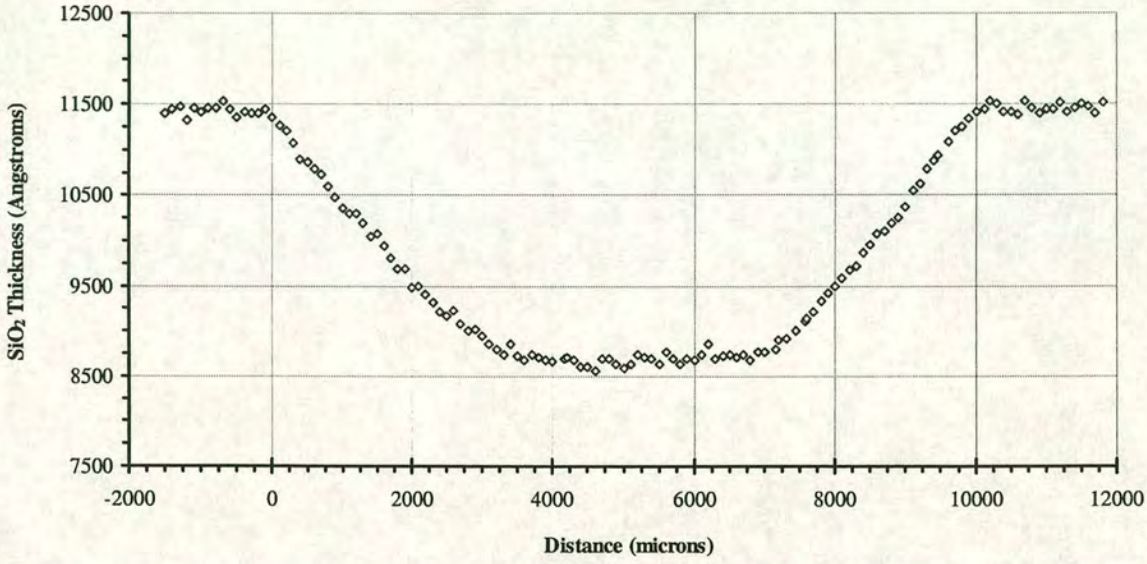


Figure 4.13 Oxide thickness after CMP with SH_{AE} = zero

When SH_{AE} is level with the field area, prior to CMP, a dished shape array results. This stems from the fact that the array has a different feature density (~56%) compared to the field oxide density (100%). This feature density difference causes the array to polish faster therefore causing dishing of the array, which is little improvement on the original post CMP domed profile.

4.4.1. Different Pre-CMP Etch Step Heights

It is interesting to note that the amount of array dishing in Figure 4.13, 0.3μm is approximately the same as the amount of doming (0.3μm) in Figure 4.9. This is probably a coincidence but an important insight may be learned. If the array is etched, pre-CMP, to such a SH_{AE} that the doming, caused by pad deformation, and dishing, caused by different feature densities, may be made to cancel each other out.

To establish the correct SH_{AE} a series of wafers were polished with a range of step heights. The step heights chosen were 0.4μm, 0.6μm, 0.8μm and 1μm. As the number of wafers available were limited it was decided to run two step heights on each wafer. To achieve this half of the wafer was covered for the first part of the etch then exposed for the correct time.

Step Height	Etch time (@ 25nm/ min)	Wafer #1
0.4μm	44 minutes	Etch for 8 minutes
0.6μm	36 minutes	Uncover etch for 36 minutes
0.8μm	28 minutes	Etch for 8 minutes
1.0μm	20 minutes	Uncover etch for 20 minutes

Table 4-2 Etch time for wafers in the pre-CMP etch tests

Again, as the measurements needed to establish uniformity were very time consuming, visual inspection was initially used. It could be seen that a step height of 0.8μm produced virtually no fringes while all other step heights had fringes of various degrees. Once the visual inspection had ascertained that the best SH_{AE} was 0.8μm the test pattern was measured. The results can be seen in Figure 4.14.

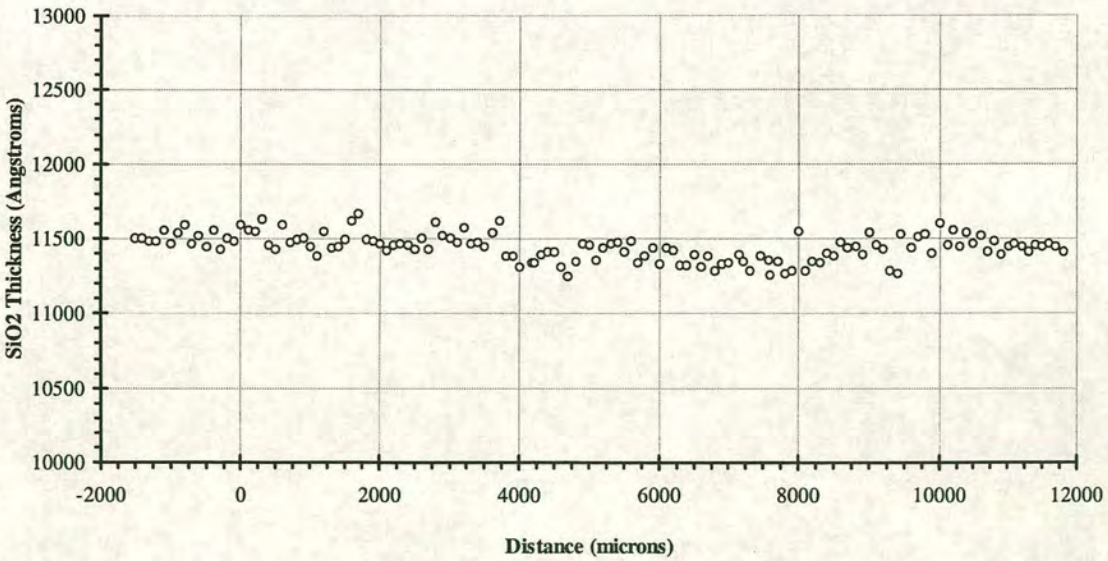


Figure 4.14 Oxide thickness uniformity after CMP with SH_{AE} = 0.8μm

It can be seen from Figure 4.14 that the oxide thickness is now far more uniform without any sign of doming or dishing. The standard deviation for the oxide over the 10mm array area is 10nm. The surface features have been completely removed as has the array step height as shown in Figure 4.15 and Figure 4.16.

Figure 4.15 Photomicrograph of cross section of edge of test pattern after CMP

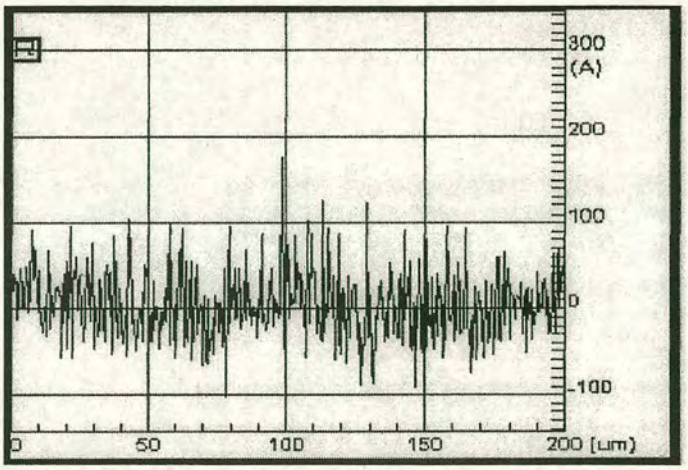


Figure 4.16 Surface profile trace of edge of test array after CMP

4.5. Conclusions and Comments

The use of CMP to remove circuitry induced topography on commercially supplied wafers proved a difficult challenge. The main problem was associated with the large array mesa which was ≈1.6μm above the field area. After CMP the mesa was reduced to a dome shape whose center was 0.3μm above the field region. A pre-CMP array etch was used to reduce the initial mesa height. It was found that etching the array level with the surrounding field area produced a

dished shape array of about 0.3μm in depth. The array step height was etched to a height that resulted in the domeing effect being cancelled out by the dishing effect resulting in a uniform oxide thickness across the array. The ideal pre-CMP array step height was found to be 0.8μm. This produced an oxide thickness uniformity with a standard deviation of only 10nm. Comparison of the post CMP profiles produced by array step heights of 1.6μm, 0.8μm, and 0μm can be seen in Figure 4.17

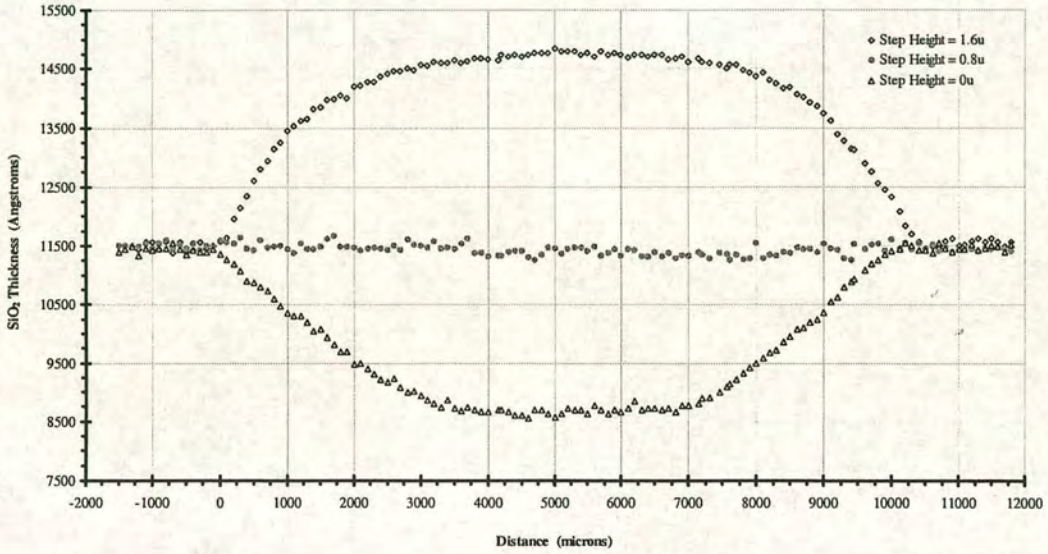


Figure 4.17 Graph comparing post-CMP array profiles

It must be emphasised that the tests were carried out on a test pattern which were designed to mimic the real device topography as close as possible. An exact match was impossible so some difference in feature density between the real device and test pattern can be expected. This may result in the real device behaving differently during CMP. Although 0.8μm was found to be the optimum pre-CMP step height for the test pattern some modification of this may be needed to produce a similar uniform removal rate across a real device array.

An important aspect of CMP has also been highlighted. This is that once a polish profile has been established it will not be removed by further polishing. This level of planarisation is the fundamental limit which this set of process (and

consumable) variables can achieve. It may be possible to improve the polish uniformity still further, but to do this a new consumable set is needed, which was not available during this study.

5. Metal Chemical Mechanical Polishing

Metal CMP is also called the damascene process; this is because a technique of inlaying metal was developed in the city of Damascus, Syria, at around 64BC. This process involved inlaying one metal into another and was done, most notably, in swords where gold was inlaid into the iron blades as a form of decoration.

The application, and technique, is now much altered but it still involves inlaying one material within another. The term is now more usually applied to the technique whereby conductive metal features are imbedded within, and level with, the surface of an insulating material.

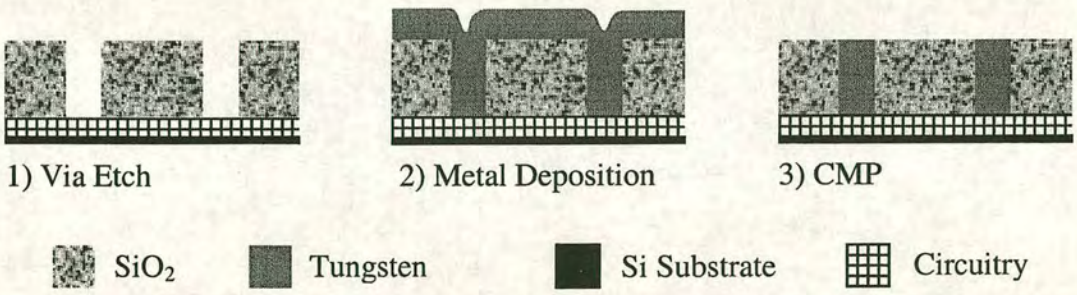


Figure 5.1 Schematic of metal via CMP (damascene)

The first inlaid metal patterns to be used by the microelectronics industry were tungsten studs[72], as shown in Figure 5.1. The metal pattern is first etched into the planarised dielectric film (metal CMP must be preceded by a dielectric planarisation step), metal is then deposited to a thickness sufficient to fully fill the vias. The tungsten overburden is then removed leaving the metal features buried within the dielectric.

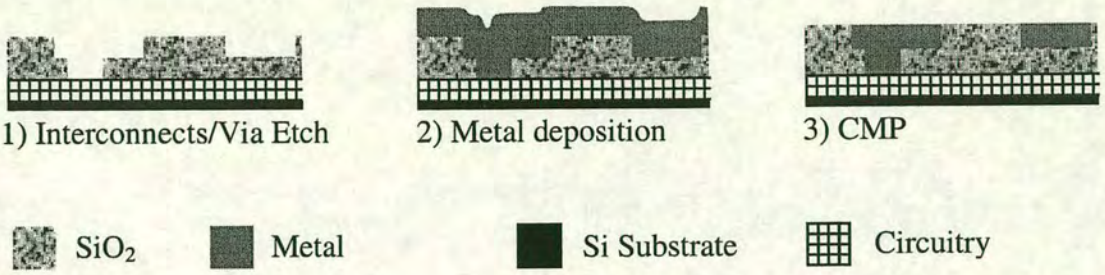


Figure 5.2 Schematic of metal interconnect/via CMP (dual-damascene)

This technique can be carried a stage further with not only the inter-metal contacts being defined by CMP but also the interconnects[73], Figure 5.2. This results in a fully planarised surface. With the advent of copper, metal CMP has become much more important[74] as it is difficult to pattern copper using conventional methods.

The following chapter is divided into two sections. The first explains the mechanism by which planerisation of metal is achieved, the second highlights some of the problems associated with metal CMP and explain their origins.

Of course many of the process variables and consumables are the same as those used in dielectric CMP. The major difference being the slurry and possibly the pad, which are the two most important parameters in virtually all aspects of CMP.

5.1. Chemical Processes in Metal CMP

Metal CMP is a far more complex process than dielectric CMP. It does, however, work on the same basic principal, that of chemical surface modification followed by mechanical abrasion. With SiO_2 the 'active' chemical component in the slurry is water while in metal CMP it is usually a far more complex solution of passivation and etching agents. It is even more complex because each metal has different chemical and mechanical characteristics, and as such each needs its own specific slurry 'recipe'. In this thesis only the CMP of aluminium will be

investigated, although many of the principles apply equally well to other metals.

Kaufman *et al*[75], and also Wang *et al*[76], proposed a metal CMP model which breaks the removal process down into separately defined stages. The surface is first chemically modified, usually by an oxidant, this oxide is then mechanically abraded by the particulates within the slurry. Planarisation is achieved by the oxide primarily being removed from the high areas, Figure 5.3. These high areas are subject to more applied pressure from the polishing pad, as such they experience a greater degree of mechanical abrasion. The low areas are protected from physical abrasion and from chemical attack by the presence of the passivating layer.

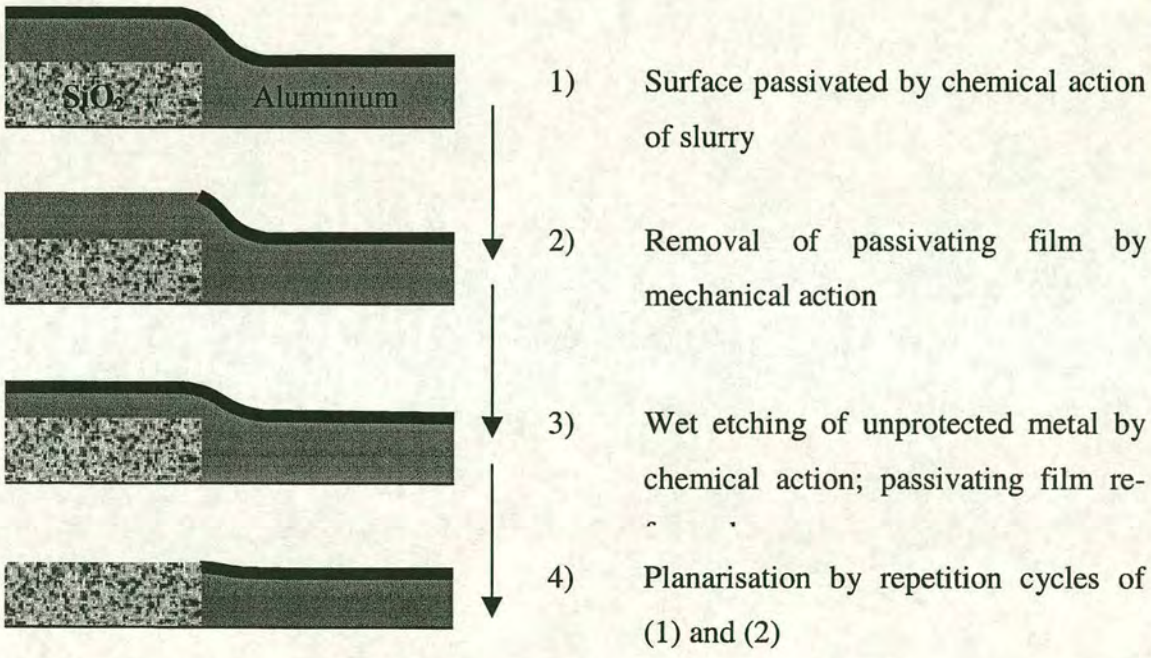
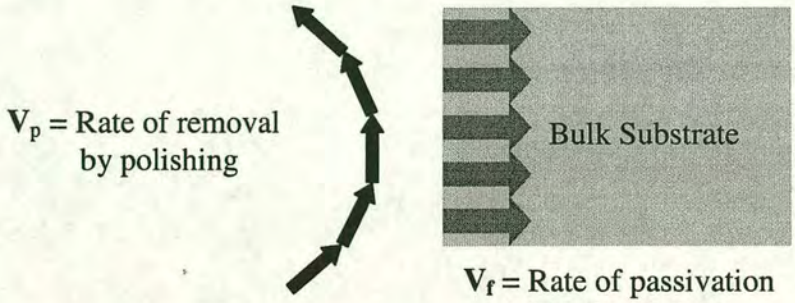


Figure 5.3 Schematic representation of metal removal by CMP[77]

Continuos cycles of formation, removal, and re-formation of the passivating layer continue until the final thickness of metal is achieved. At the same time because of the non-equal polishing rates between high and low areas planarisation also occurs.

It is obvious that the speed of surface passivation is critical in achieving, not only optimum removal rates, but also good surface finish. There needs to be a careful balance between the chemical and mechanical components of the polishing process, see Figure 5.4

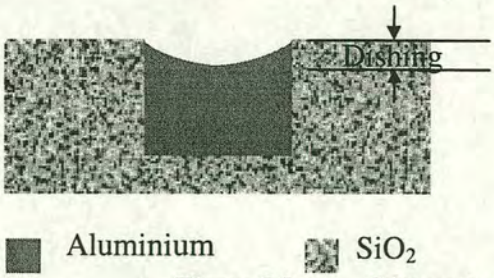


1) $V_f > V_p$ Stable passivation layer during CMP, low CMP rate
2) $V_f = V_p$ Clean surface, maximum CMP rate
3) $V_f < V_p$ Clean surface, low CMP rate

Figure 5.4 Diagrammatic representation of the polishing process[78]

5.2. Dishing

Feature dishing is one of the main problems associated with metal CMP, Figure 5.5. Dishing is undesirable because it lessens the planarity of the final polished surface, but more importantly reduces the final interconnect thickness. If the CMP process is not sufficiently optimised it can also lead to different track thickness across the device due to uneven wafer scale polishing rates.



For a given feature dishing is defined as the difference in height between the center of the feature, which is usually its lowest point, and the point where the SiO_2 levels off, which is the highest point.

Figure 5.5 Schematic representation of feature dishing

Dishing can be induced by four different phenomena; pad deflection[79], pad asperities[80], particulate bombardment[81] and chemical etching[82].

5.2.1. Pad deflection

In this mode dishing is the result of the pad being deflected by the applied load. It is forced into the feature cavity (formed by the conformal filling of the feature) at the beginning of the polishing cycle. This deflection profile then continues until the pad contacts the top of the feature. As the polishing rate is the same both at the surface and the top of the feature the profile created by the initial feature depression is maintained throughout the polishing cycle, Figure 5.6.

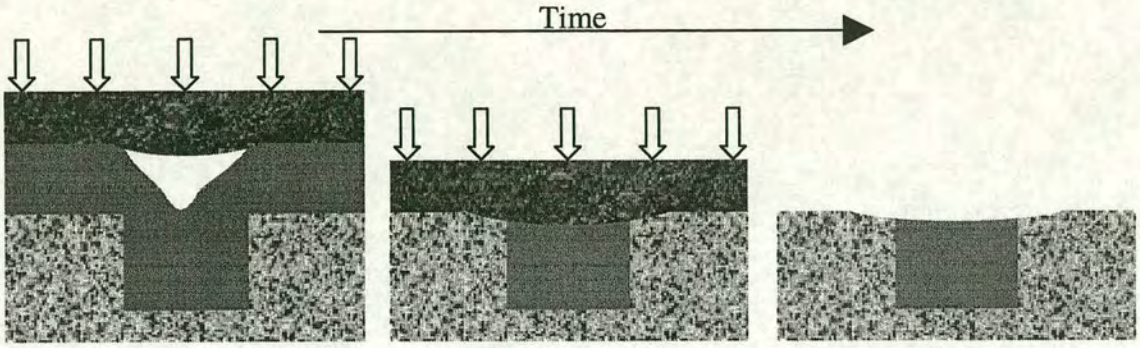


Figure 5.6 Schematic of Dishing caused by pad deflection into 'filling void'

Sivaram *et al*[79] suggested that the deflection of the pad may be explained using a bending beam model. The maximum deflection of the pad (measured at the centre of the recess) is given by:

$$y = \frac{5wL^4}{32Et^3}$$

Equation 5-1 Deflection of a pad, under load, into a recess[83]

w is the applied load
E is the modulus of Elasticity
L is the width of the recess
t is the pad thickness

Equation 5-1 is a somewhat oversimplification but it indicates the important parameters that affect dishing. In particular it suggests that the amount of dishing, equal to the pad deflection, increases with feature width (L). In addition dishing decreases with decreasing applied load (w) and as the modulus of elasticity (E) of the pad increases.

5.2.2. Pad Asperities

During CMP the wafer interacts with the top tens of microns of the pad surface. It is apparent that the surface properties of the pad will influence the amount of dishing, Figure 5.7. The lateral and vertical dimensions of the pads surface asperities play a prominent role. Features smaller than the asperity are not affected by this form of dishing, as the asperity is unable to penetrate the feature.

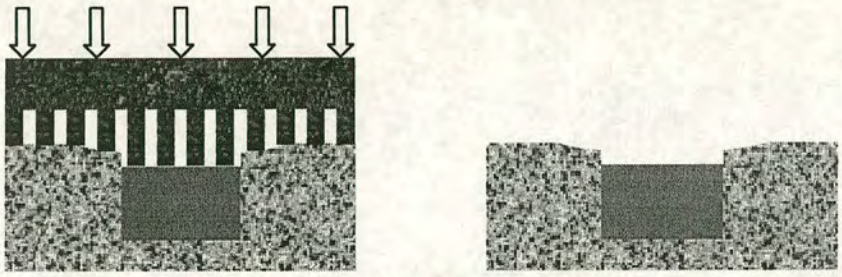


Figure 5.7 Schematic of Dishing caused by pad asperities

5.2.3. Particulate Bombardment

As the wafer is polished hydrodynamic effects occur within the slurry. As with SiO_2 CMP the removal mechanism is a combination of asperity contact and fluid based turbulent erosion. In metal CMP it is thought that it is fluid based erosion that predominates, because excessive wafer/pad contact results in scratching. The slurry is caused to become turbulent by a combination of the relative motion of the pad and wafer and by the surface roughness of the pad. The particulates, within the slurry, are caused to impact the wafer surface by the motion of the slurry. These particles posses enough kinetic energy to abrade the surface material, Figure 5.8. As features are initially below the surface this causes the slurry to

'eddy' in these regions. This leads to enhanced particulate bombardment, and material removal, on the top surface of the incompletely filled feature.

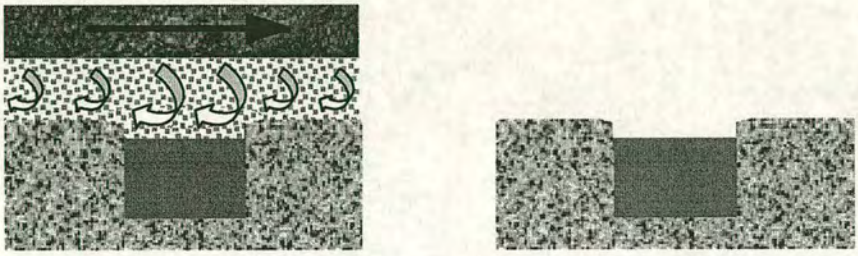


Figure 5.8 Schematic of Dishing caused by particulate bombardment

As a certain amount of over-polish may necessary, due to poor wafer scale polish uniformity, this also contributes to dishing. Once the blanket aluminium has been removed the particles impact the SiO_2 with the same energy as the aluminium, because the aluminium is softer than the SiO_2 it is abraded faster leading to increased dishing of the feature.

5.2.4. Chemical Etching

As metal CMP is very chemical in nature a careful balance of the slurry properties has to be achieved. The slurry will attack the unprotected aluminium if the passivation layer is not reformed sufficiently quickly, Figure 5.9.

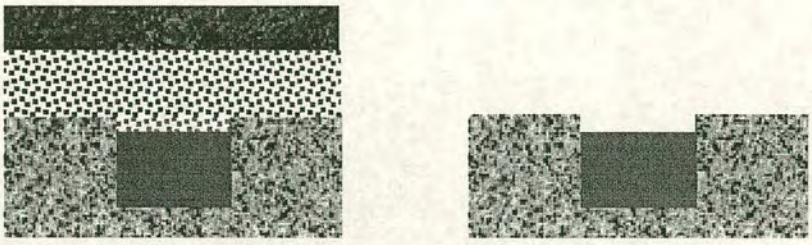


Figure 5.9 Schematic of Dishing caused by chemical etching

As this is a chemical process it is strongly dependent upon the temperature of the slurry, higher temperatures leading to higher chemical activity. Chemical etching is characterised by straight sidewalls and a flat top feature.

5.2.5. Feature Profile

Of course it would be a simplistic view if the feature dishing observed could be attributed to one particular cause. In realty it is a combination of all the different phenomena mentioned above. Thus the final shape, seen in Figure 5.10, is a complex profile evolved from the various wafer/pad/slurry interactions.

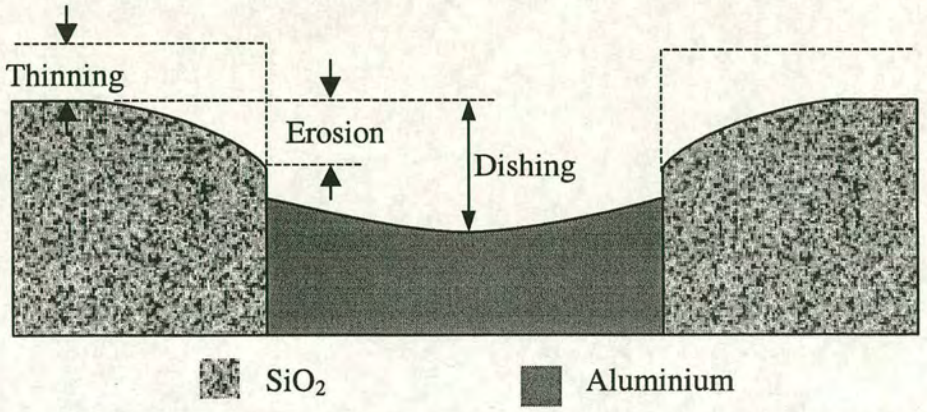
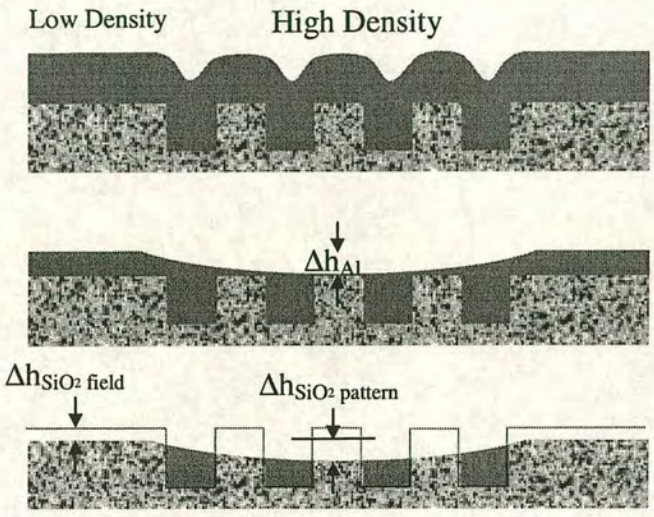


Figure 5.10 **Generic features of a polished pattern that may arise as a result of CMP[84]**

5.3. Erosion

Erosion is the term used to describe the amount of unwanted SiO_2 removal found after metal CMP, Figure 5.11. It is a direct consequence of the non-zero polish rate of SiO_2 during metal CMP.



Regions of high and low feature density

Aluminium polishes faster in high pattern density areas exposing underlying SiO_2

SiO_2 receives more polishing time in regions of high pattern density causing erosion

Thinning is defined as the difference in the SiO_2 thickness before and after the polish step:

$$\Delta h_{SiO_2\ field}$$

Erosion is defined as the difference between the lowest point within the pattern and the 'new' field surface:

$$\Delta h_{SiO_2\ pattern}$$

Figure 5.11 Schematic of the cause of dielectric erosion (dishing is not shown)

High feature dense areas experience more localised pad pressure than low-density areas. This is because pressure is a function of area and as high-density areas have less 'up' area they experience an increase in localised polishing pressure. This leads to a higher removal rate, which clears these areas of metal first thereby exposing the underlying SiO_2, Δh_{Al}, shown in Figure 5.11. Once

exposed, the SiO_2 is then subject to the polishing action of the pad, because of the non-zero SiO_2 polish rate this leads to erosion, $\Delta h_{SiO_2\ pattern}$

The field region also experiences SiO_2 loss, due to non-uniform wafer scale polishing, $\Delta h_{SiO_2\ field}$ in Figure 5.11. This is also termed die thinning. The total erosion after polishing is a combination of $\Delta h_{SiO_2\ field}$ and $\Delta h_{SiO_2\ pattern}$.

5.4. Scratching And Surface Finish

Scratching can be caused by several factors although slurry particulate agglomeration is perhaps the main one. Metal slurries are not colloidal solutions and have a tendency to 'settle out' if they are not continually agitated. This causes the particulates to adhere together, a slurry with a nominal particulate size of 50nm can contain agglomerated particulates many microns in size[85]. These large particulates can lead to scratches hundreds of nanometers in depth and tens of millimetres in length. Other smaller or micro-scratches, tens of microns long, can be caused by abraded material. The abraded material, if not dissolved by the slurry, can become lodged within the pad matrix. As more collect they can agglomerate and lead to scratches. This can be a particular problem with aluminium because the abraded material (thought to be Al_2O_3[86]) is far harder than the aluminium.

5.5. Particulate Contamination

Post CMP contamination is now becoming a major concern especially as geometries continue to shrink. CMP has always been a double-edged sword. Vast amounts of time, effort and money are expended in maintaining high class cleanrooms, in order to keep wafer particulate contamination at extremely low levels. These clean wafers are then exposed to a process where sub-micron sized particles are used in their billions. The once clean wafers are no longer. The cleaning methods are as varied and complex as CMP itself[87,88] and as such a whole industry has emerged to service this need.

5.5.1. Summary

In practice dishing is caused by a combination of several, or even all, of the phenomenon previously described. It would be very difficult isolate the contribution made be each type to the amount of dishing observed.

One of the main influences of dishing and erosion is that of wafer scale polish uniformity. If the uniformity is poor it will result in areas of the wafer experiencing a long over-polish time[89]. This will increase the severity of all the types of dishing discussed.

In Table 5-1 the four types of dishing are listed along with the process variables which they have most dependence upon. Erosion is also a direct result of over-polish, either in closely packed features or on a die or wafer level.

	Dishing Mode						
Process Variable	Pad Deflection	Pad Asperities	Particulate Bombardment	Chemical Etching	Erosion	Scratching	Contamination
Platen Speed	5	4	10	1	2	1	1
Head Speed	5	4	10	1	2	1	1
Head Pressure	10	8	5	1	2	5	1
Back Pressure	8	5	5	1	2	5	1
Feature Size	10	10	10	1	4	2	1
Particulate Size	1	1	10	1	2	8	5
Slurry Chemistry	1	1	2	10	10	10	8
Pad Hardness	10	5	5	1	7	9	1
Pad Roughness	1	10	7	1	7	8	1
Pad Conditioning	4	8	5	1	7	8	1
Over-polish Time	8	8	8	5	10	2	1
Temperature	8	8	2	10	6	5	1
Post CMP Clean	1	1	1	1	1	5	10
Highly Dependent 10 9 8 7 6 5 4 3 2 1 Little Dependence							

Table 5-1 **Table showing dependence of different dishing mechanisms with process variables**

5.6. Conclusions and Comments

When looking at the layout of a SLM it is apparent that it contains an area of high feature density, the array, surrounded by an area of low pattern density, the field. This will lead to severe erosion within the array. As mentioned in Chapter 1 the main reason for using the damascene process, in the post processing sequence of SLMs', is to produce mirrors which are level with the dielectric surface. This will allow the LC to flow across the array unperturbed while filling, leading to better LC alignment. It is therefore obvious that any departure from a truly planar surface will have a detrimental effect on LC alignment quality. Erosion, being on a larger length scale, will also affect the cell gap uniformity leading to optical colour fringes in the device. Dishing will have the effect of producing 'walls' around each mirror pixel causing a further disturbance in the LC fill flow front.

Surface finish is also important. Whereas in IC production scratches can lead to localised interconnect thinning or, even worse, breakage causing device failure. For SLM devices the surface finish will have a direct effect on the optical performance, with only minor effect upon the electrical performance.

Surface finish has, however, a direct effect on reflectivity, Equation 5-2, the lower the surface RMS value the higher the reflectivity (or lower scattering), all other things being equal.

$$TIS \cong \left(\frac{4\pi\delta}{\lambda}\right)^2$$

Equation 5-2 **After [90] Where TIS is the total integrated scattering and δ is the RMS height of the surface irregularities and λ is the wavelength of light**

6. Test Pattern for Metal CMP

To better understand the mechanisms involved in the CMP of aluminium, a test structure was designed. The purpose of the structure was to investigate the effects of process and consumable set variables on dishing and erosion. The pattern consisted of various line width and pitch structures which enabled the investigation of the link between feature size and density with dishing and erosion. The test pattern can be seen in Figure 6.1

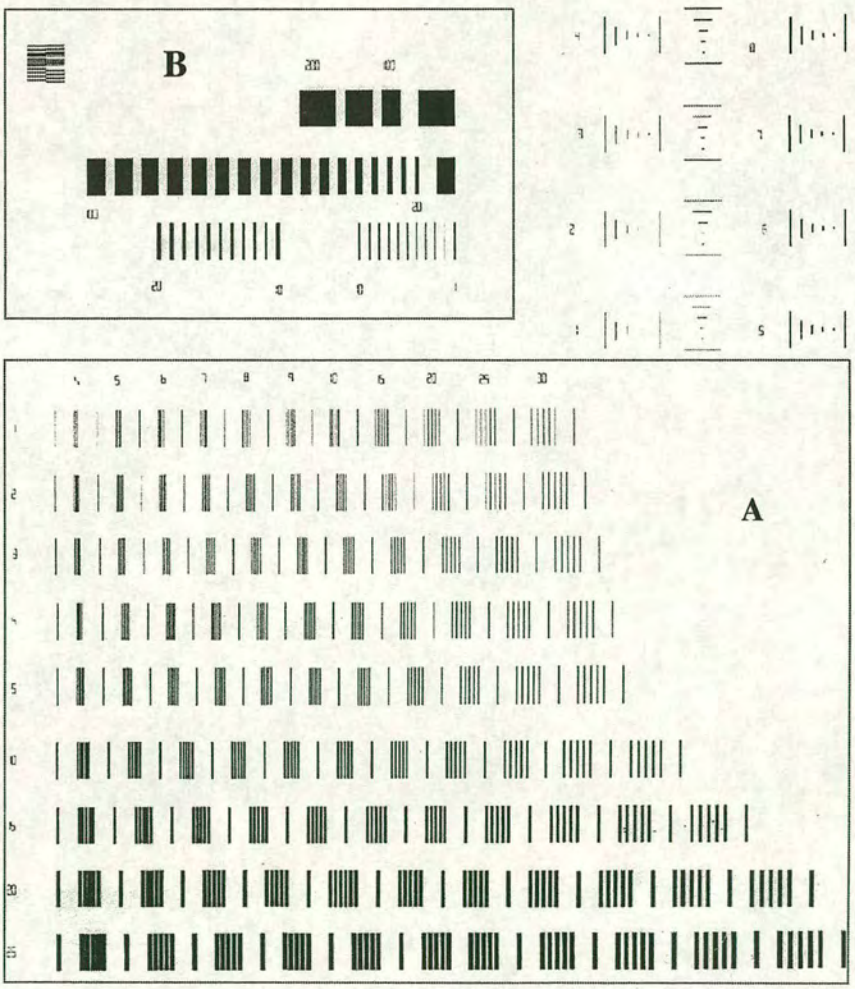


Figure 6.1 Test pattern used in the CMP tests. (designed by K. Seunarine)

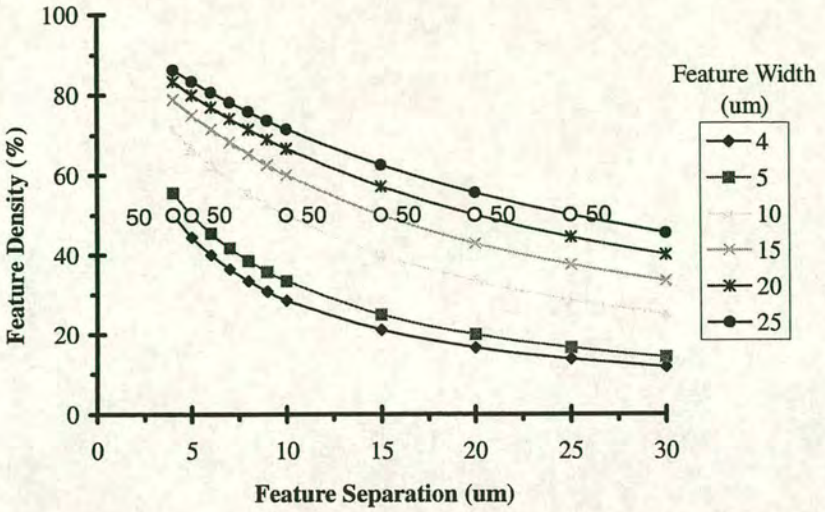


Figure 6.2 Range of feature densities in the test pattern

The pattern consists of groups of five 200μm long features, Figure 6.1A. which range from 1 to 25μm in width and are separated by between 4 and 30μm The range of pattern densities within the test structure is from 11% to 86%, Figure 6.2. There is also a set of single features, again 200μm long, ranging from 1 to 200μm wide, Figure 6.1B. This pattern was etched into 0.5μm of ECR SiO_2 which was deposited onto 75mm wafers, 1.5μm of aluminium was then sputter deposited to ensure complete filling of the 0.5μm deep features.

6.1. Tests Using Polytex Pad

From previous experience on the old Logitec polisher it was decide to use a soft pad in the initial tests; the actual pad used was a Rodel 'Politex Supreme Embossed'. This pad is made of a black chemically blown polymer with a grid pattern of grooves, spaced approximately 2mm apart, to aid slurry transport under the wafer. It is a softer pad (Shore D hardness of ~34, Rodel) than the IC1000 (Shore D hardness~57, Rodel) with a single layer construction. Being softer it was thought that it would be less likely to scratch the aluminium. SEM images of the pad can be seen in Figure 6.3.

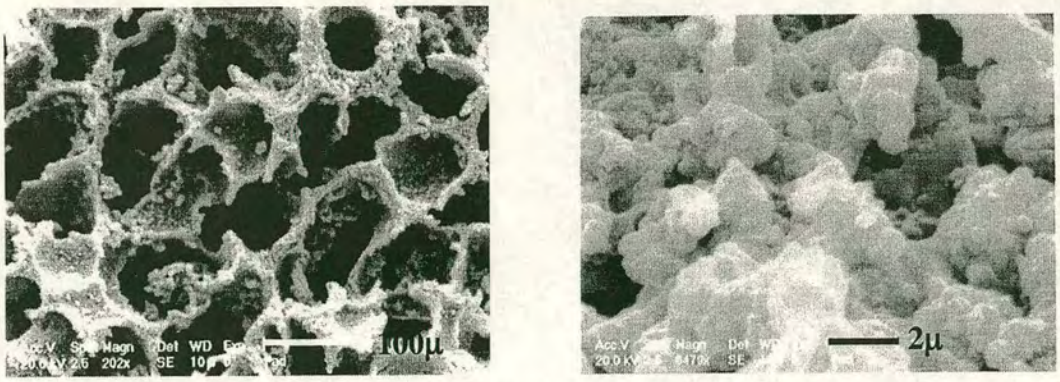


Figure 6.3 SEM images of surface of Polytex supreme pad

It can be seen that the pad is extremely porous with a sponge like texture, containing voids approximately 50µm in size. The material surface is textured with small, ≈1µm, features which are thought to aid in trapping the abrasive particles, while the large voids help in slurry transport under the wafer. The slurry used was Rodel QCT1010 with 30% H_2O_2 as the oxidising agent (as recommended by Rodel), the process variables used can be seen in Table 6-1.

Parameter	Setting
Head Speed	30 rpm
Table speed	30 rpm
Head pressure	1 bar
Back pressure	0.3 bar
Slurry flow	150 ml/min
Temperature	15°C

Table 6-1 Process variables use in the Polytex pad tests

The damascene test pattern contained features from 25µm to 1µm wide, with spacing ranging from 30µm to 4µm. As access to an AFM was not possible a Dektak surface profilometer was used to asses CMP-induced dishing and erosion. It was found that features less than 5µm in width could not be resolved to their full depth using the 5µm diameter stylus (see Appendix A). This made it impossible to determine the full extent of dishing in these features and so make it

difficult to compare the effect of the process variables on dishing of the smaller features.

6.2. Results Of Polytex Pad Tests

The results of the tests can be seen in Figure 6.4, to Figure 6.8

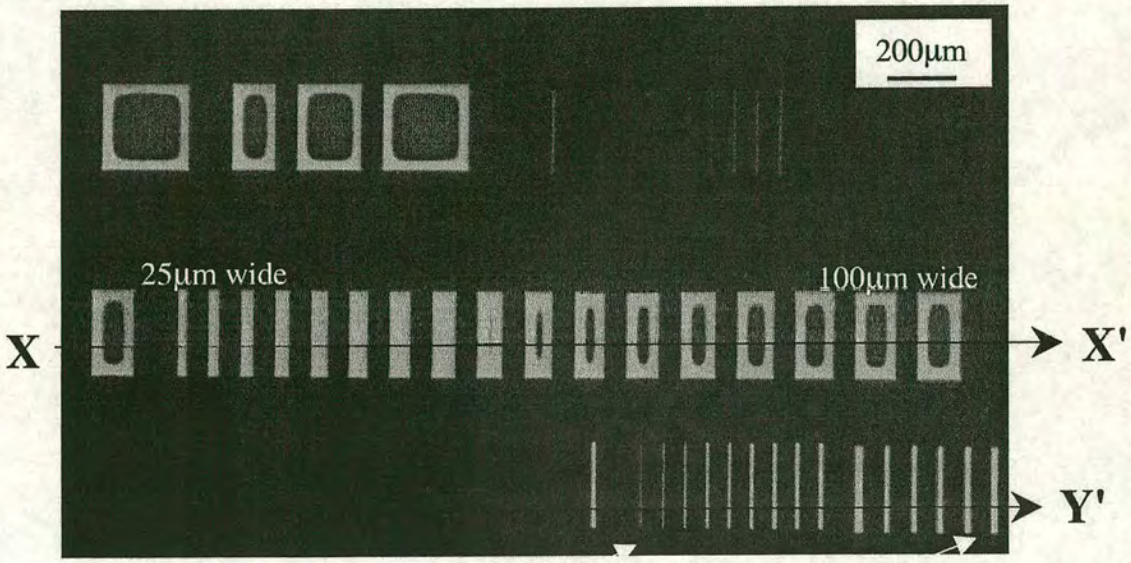


Figure 6.4 Opticalmicrograph showing dishing of features.
(The dark areas in the wide features are the underlying silicon wafer)

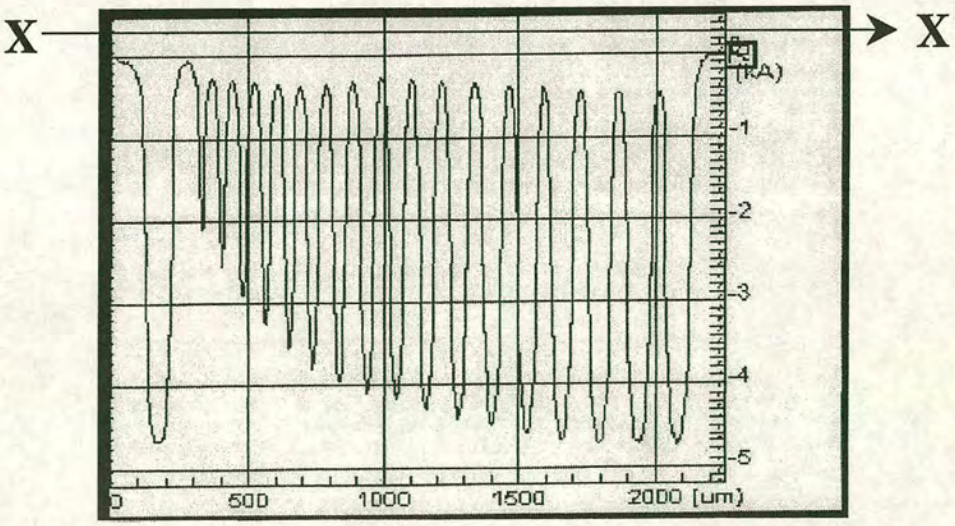


Figure 6.5 Surface profile trace along XX' of Figure 6.4

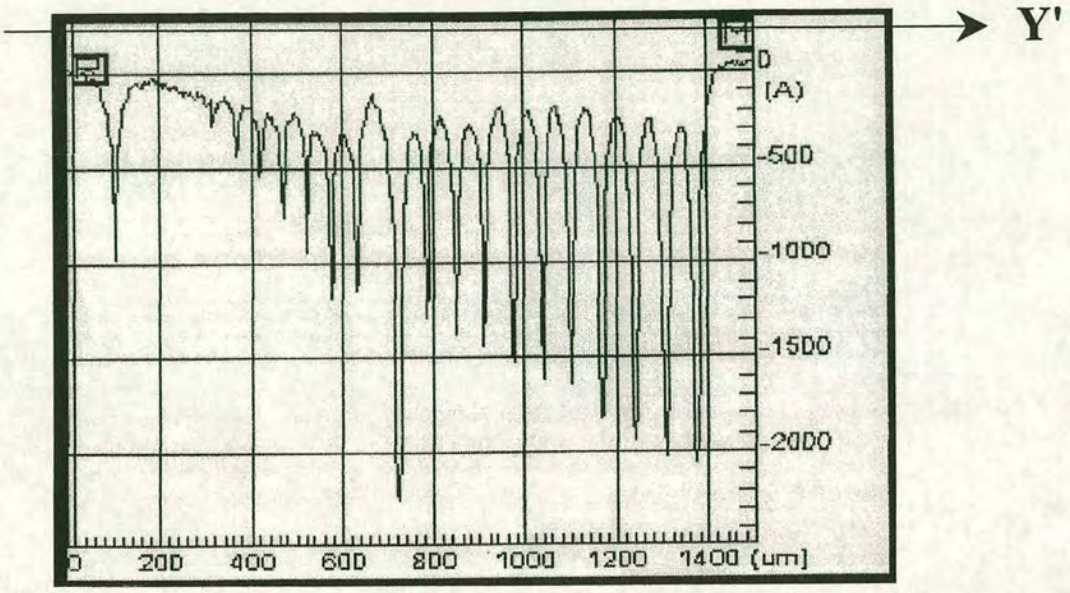


Figure 6.6 **Surface profile trace along YY' of Figure 6.4**

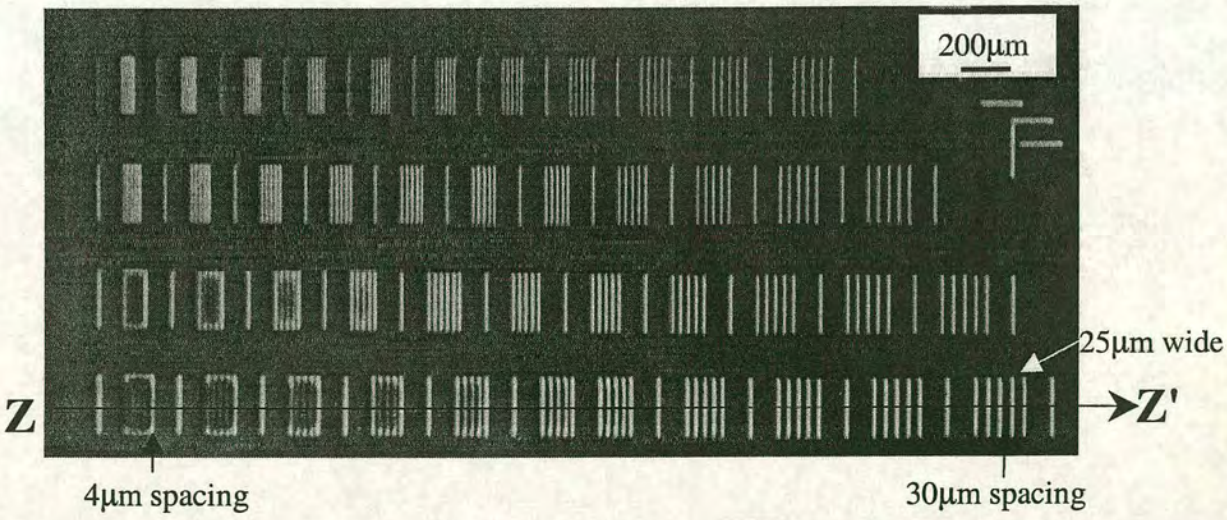


Figure 6.7 **Optical micrograph showing dishing and erosion**
(The light areas are aluminium features)

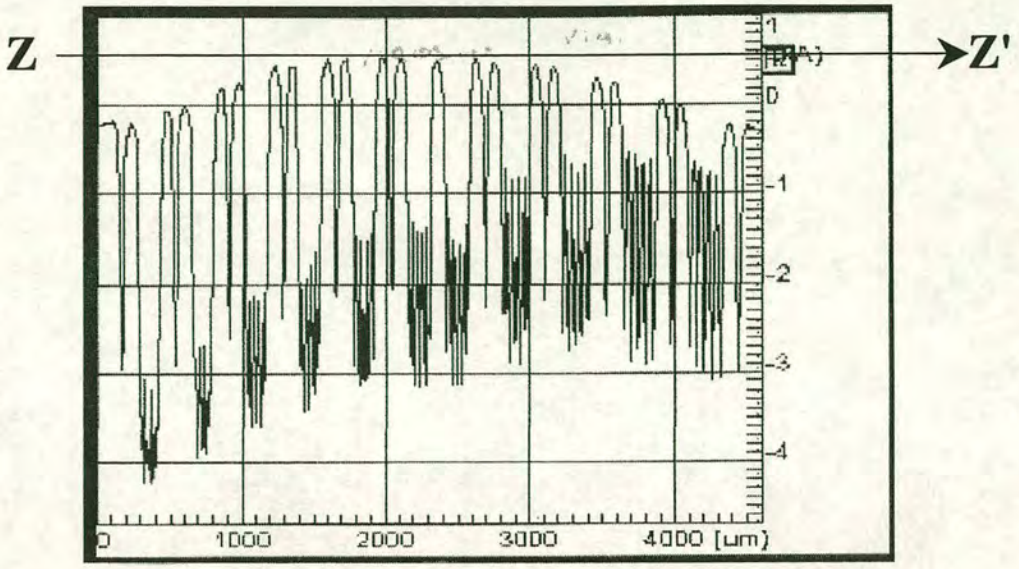


Figure 6.8 **Surface profile trace along ZZ', 25μm track width of Figure 6.7 (The gross curve in the trace is due to wafer-warp)**

It is clearly evident that gross dishing and erosion has occurred, this is caused by the extreme compliance of the pad. As the wafer is pressed against the pad, the pad surface is easily deformed[91] into the feature cavities. This allows the pad to remove material from the feature bottom as well as the wafer surface, resulting in poor planarisation. As seen in the surface profile traces in Figure 6.5, Figure 6.6 and Figure 6.8, some degree of planarisation does still occur but only for narrower features. This is thought to be because the pad is unable to 'penetrate' into these features, see Figure 6.9. The surrounding SiO_2 'supports' the pad as it spans the feature. As the feature width increases, this support has a lessened effect. The result is the pad penetrates the wider features more readily than the narrower ones.

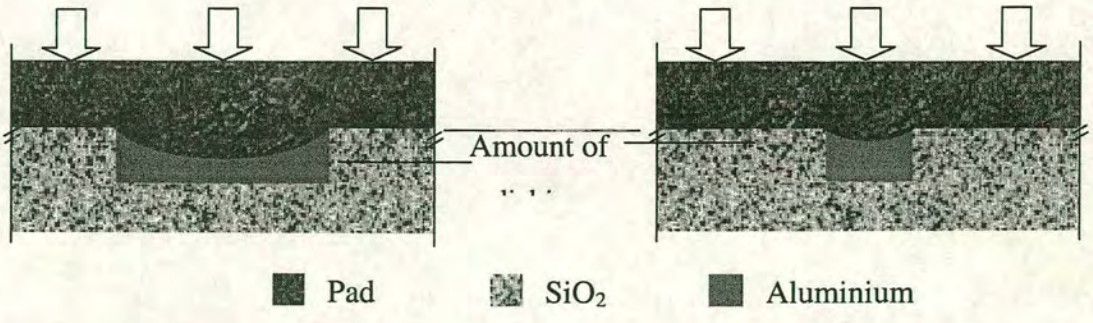


Figure 6.9 **Schematic showing pad penetration of different size features.**

The feature dishing is so severe that the aluminum has been completely removed in the centre of features 60μm wide and over, Figure 6.4 and Figure 6.10. However, for smaller features some degree of planarisation is apparent with dishing of ≈120nm for the 10μm feature.

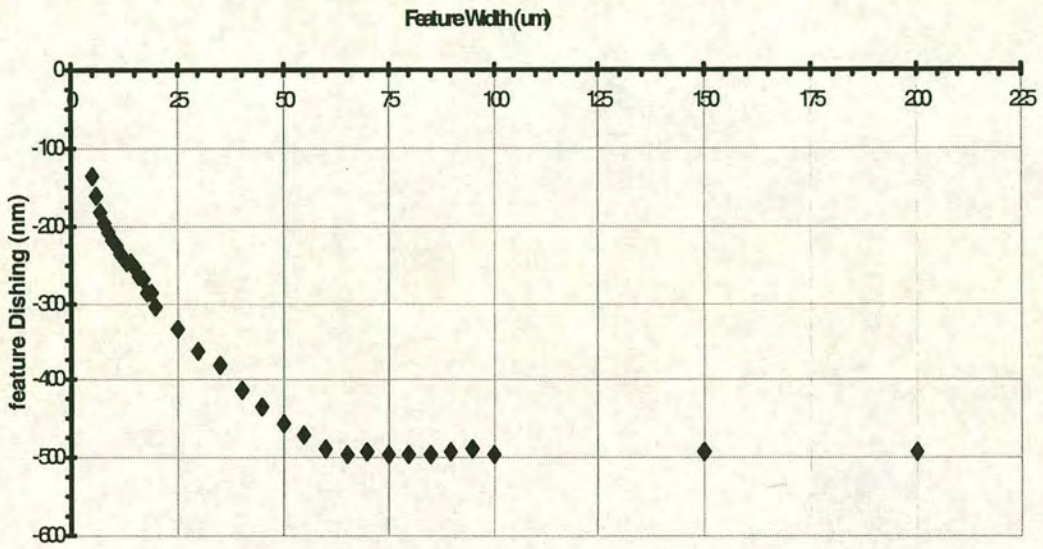


Figure 6.10 Graph showing amount of feature dishing using Polytex pad

As observed in Figure 6.10 the amount of dishing is a strong function of feature width. Once the aluminium overburden has been removed the features become isolated and surrounded by SiO_2. A certain amount of over-polish time is then necessary to ensure all areas of the wafer are cleared of the aluminium overburden because of poor wafer scale polish uniformity.

The pressure exerted on the aluminium remaining within the features, by the pad, is now the same as that on the surrounding SiO_2, aluminium, being softer, polishers faster. As the aluminium is abraded from the features so the pressure exerted by the pad lessens (the pad becomes 'supported, by the surrounding SiO_2). When a critical depth is reached this reduced pad pressure lowers the removal rate and equilibrium is achieved. The pressure exerted by the pad in the bottom of the feature is less than that exerted on the surrounding SiO_2. The difference in

material hardness is now cancelled out by the difference in polishing pressures (as polishing rate is a function of polishing pressure). Obviously, the stiffness of the pad plays an important role, for this governs its ability to be deformed under the applied load, hence a softer pad generates more feature dishing.

Equation 5.1 assumes that there is no material within the feature so does not take into account the upward pressure applied by the material within the feature which tends to support the pad. It will therefore tend to predict higher dishing than is actually observed.

Pad hardness also plays an important role in wafer scale polish uniformity. Unlike the IC1000 (used in SiO_2 polishing, Chapters 3 and 4) the Polytex pad is of a single layer construction. It results in not only the surface being compliant but also the bulk material of the pad. This allows the soft pad to deform easily to the wafer shape, resulting in a uniform pressure across the entire wafer surface. Wafer scale uniformity is more critical in metal polishing than dielectric polishing. If the dielectric is polished non-uniformly it results in different via contact etch depths. If the damascene process is non-uniform it results in over-polish of certain areas. This over-polish causes increased dishing and erosion which can lead to different interconnect thickness.

It is not only dishing which is observed to be severe, but also dielectric erosion, as can be seen in Figure 6.8. The amount of SiO_2 erosion, for 25μm tracks, spaced at 30μm, is approximately 80nm Figure 6.11, for 25μm tracks spaced 4μm the SiO_2 has been eroded to a depth of 280nm, Figure 6.12.

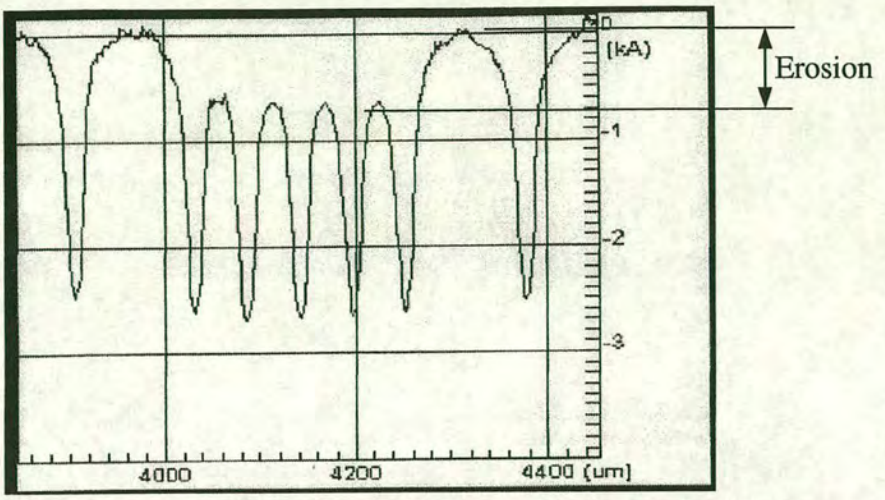


Figure 6.11 Surface profile trace of 25μm lines spaced 30μ m apart

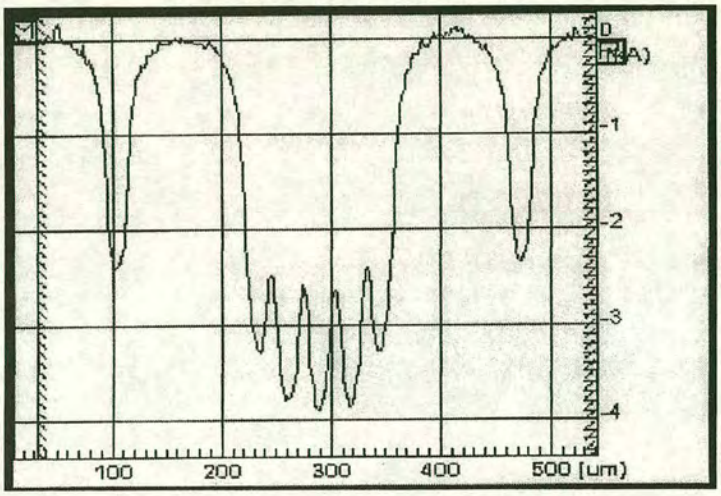


Figure 6.12 Surface profile trace of 25μm lines spaced 4μm apart

The erosion profile for the 4μm spaced features exhibits a dished shape superimposed on the erosion profile. This is because the pad 'sees' the closely spaced features as a single large feature. The 4μm SiO_2 'walls' between the features are not wide enough to support the pad load. This causes the walls to be eroded as this small contact area leads to higher localised polishing pressure and higher aluminium removal rates, exposing the underlying SiO_2 faster than the 25μm spaced features. The 25μm spaced features do not show this dished-erosion profile. The SiO_2'walls', being wider, are less prone to the erosion effects of the pad.

6.3. Hard Pad Tests

Sachan *et al*[92] suggest material removal selectivity increases with pad hardness. To investigate this an IC1000 pad was used. This is the same pad used in the CMP of SiO_2; it consists of a hard top pad stacked on compliant foam backing pad. Being harder it should not deform into the wider features giving better planarisation[93]. To assess the viability of using the IC1000 pad, blanket aluminium coated wafers were first polished. These consisted of 1.5μm of aluminium sputter deposited onto 75mm wafers which had 0.5μm of SiO_2 deposited on them.

6.3.1. IC1000 Pad Conditioning

The first wafers were polished using the same process parameters as with the Polytex pad, see Table 6-1. The results were disappointing as the aluminium surface was severely scratched. It was thought the slurry was not causing the scratching as it was the same as used with the Polytex pad. It was therefore concluded that the pad itself may be causing the problem. To prove this a blanket coated aluminium wafer was polished using only DI water the result was the same, severe scratching. The pad surface was investigated using an SEM it was seen to be composed of many large asperities, Figure 6.13. The pressures and speeds were causing the polishing to be in the Hertzian indenter regime[94] (as with SiO_2 CMP) which resulted in severe wafer/pad contact

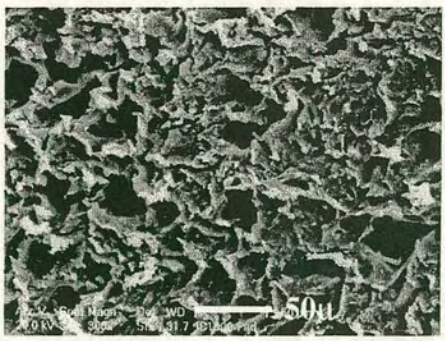


Figure 6.13 SEM of IC1000 pad surface before 'glazing'

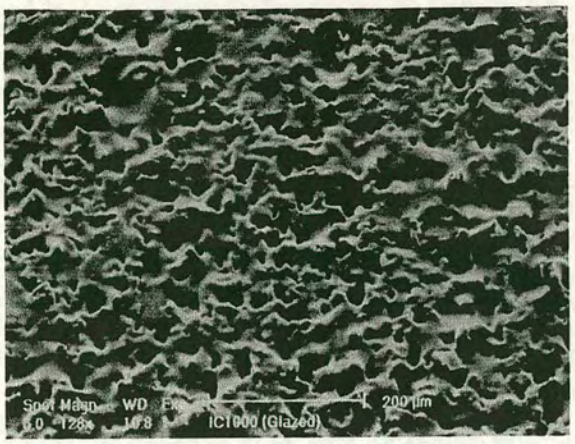


Figure 6.14 SEM of IC1000 pad surface after 'glazing'

In an attempt to transfer from an indenter type polishing regime, to a more fluid based one[94], the head and back pressures were reduced, as was the wafer and platen speed. This would help to reduce the severity of the pad/wafer contact and therefore reduce the pad induced scratching. Wang *et al*[95] suggested that selectivity is a function of polishing pressure and platen speed. It was thought this reduction in speeds/pressures should also help to decrease the amount of SiO_2 erosion.

Apart from changing the process variables, a new pad conditioning regime was developed. The normal purpose of conditioning the pad is to remove glazing and to roughen the surface to aid slurry transport between pad and wafer, it was this roughening that was causing the problem. To overcome this the pad was given a relatively long conditioning cycle (10 minutes). It was then intentionally glazed by polishing a bare silicon wafer, at high pressure and speed, for five minutes using oxide slurry (Klebosol 30H50). One minute from the end of the 'glazing' cycle the slurry was replaced with DI water in order to flush out any particulates and slurry residue from the pad surface. It was felt that it was important not to 'overglaze' the pad as this would result in poor slurry transport beneath the wafer. The aim was primarily to remove the bigger asperities, while leaving the majority of the pad surface profile intact.

It was also decided that at the end of the polishing cycle no DI water rinse would be used. This was to reduce the likelihood of any pad/wafer contact, which may be aggravated by the absence of the polishing slurry.

Several blanket test wafers were then polished using the process variables listed in Table 6-2 and Rodel QCT1010 slurry with 15% H_2O_2 as the oxidising agent. The results showed no observable scratching using the naked eye and appeared highly specular.

Parameter	Setting
Head Speed	15 rpm
Table speed	10 rpm
Head pressure	0.3 bar
Back pressure	0.2 bar
Slurry flow	200 ml/min
Temperature	10°C

Table 6-2 Process variables used in the IC1000 pad tests

The slurry flow has to be sufficient to transport abraded material off the pad and also act as a pad 'cleaning' agent. Material, which may be deposited on the pad, dissolves in the slurry and is then removed. The speed of the pad is slower than that of the wafer because it was seen that the slurry needed time to dissolve the abraded material. If the pad speed were higher this undissolved material would be transported under the wafer possibly resulting in scratching.

The time to clear the wafer of the aluminium overburden, using the above parameters was approximately 7 minutes for wafers coated with 1.5μm of aluminium.

In the absence of a post-polish DI water clean it was now necessary to clean the wafers off the machine. To achieve this the wafers were soaked in detergent for 1 minute, rinsed in DI and then spin dried. After visual inspection the wafers appeared to be free from any gross slurry residue or contamination.

6.4. Patterned Tests Using IC1000 Pad

The same test pattern was used to evaluate the IC1000 pad as was used in the Polytex pad tests, Figure 6.1. The samples were prepared in the same way, with 0.5μm of oxide being deposited followed by patterning and 1.5μm of aluminium being sputter deposited.

6.4.1. Matrix experiment

A 4 parameter, 4 level, orthogonal matrix design experiment[96] was used in order to evaluate the effect of process parameters on dishing and erosion. During the implementation of this matrix an unexpected factor became apparent, that of wafer scale polish uniformity. All wafers were observed to polish edge fast, resulting in the edge regions being over-polished in order to clear the middle of the wafer. In an attempt to counteract this, the back-pressure was increased but was seen to have little effect on polish uniformity. This is because polishing was now mainly in the fluid regime and thus an almost continuous layer of slurry exists between pad and wafer. Thus any increase in back pressure did not alter the pressure distribution on the wafer but resulted in a thinning of this slurry layer, resulting in little change in the polish uniformity, see Figure 6.15.

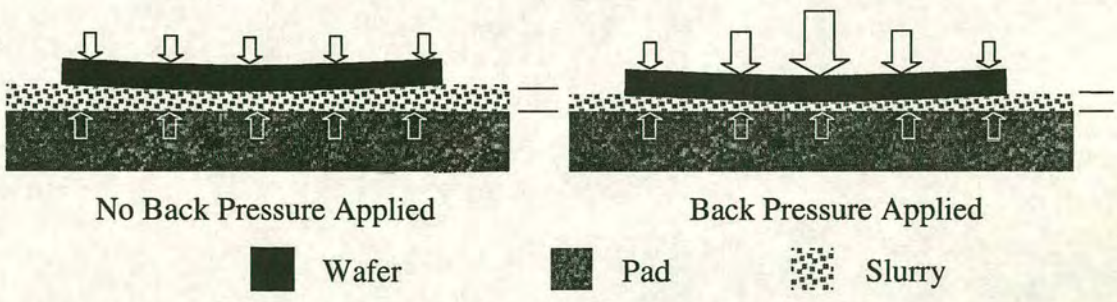


Figure 6.15 Effect of increasing back-pressure (while using low head pressure)

It was found impossible to raise the back-pressure sufficiently to overcome the natural tendency to polish edge fast. If the back-pressure was set too high it overcame the head pressure and 'blew' the wafer out of the carrier.

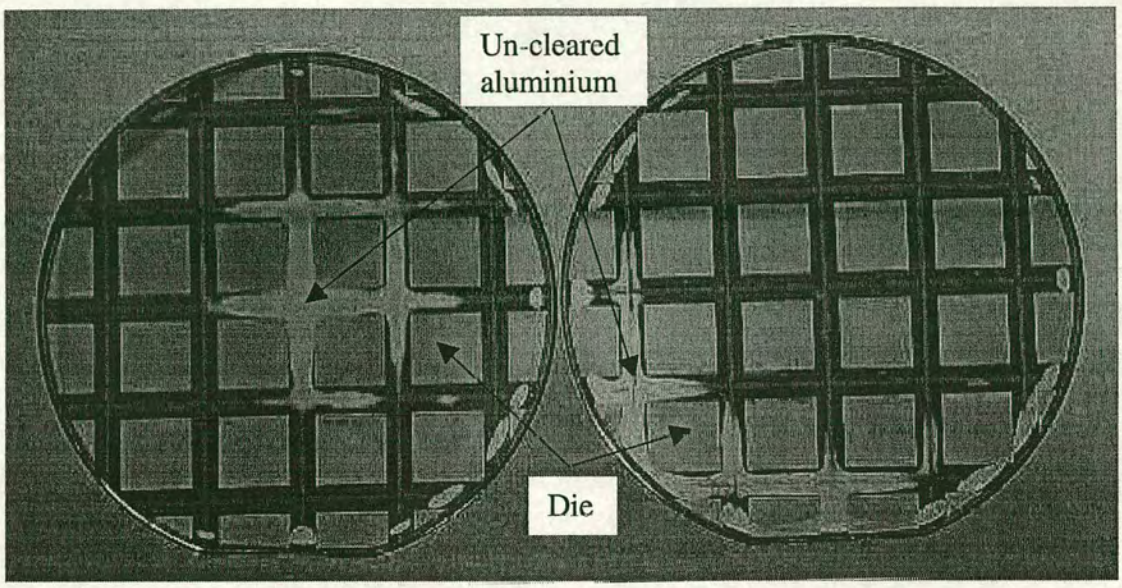


Figure 6.16 **Poor polish uniformity of two product wafers, polished with identical parameters**

The poor wafer scale polish uniformity, Figure 6.16, made it very difficult to assess the effects of the variables under investigation. The results were swamped by the larger non-uniformity effects. It was still possible, however, to investigate the effects of feature size and density on dishing and erosion. A surface profiler was used to determine the amount of dishing and erosion present after polishing.

6.4.2. Dishing

The effect of feature size and feature density on dishing can be seen in Figure 6.17 and Figure 6.18.

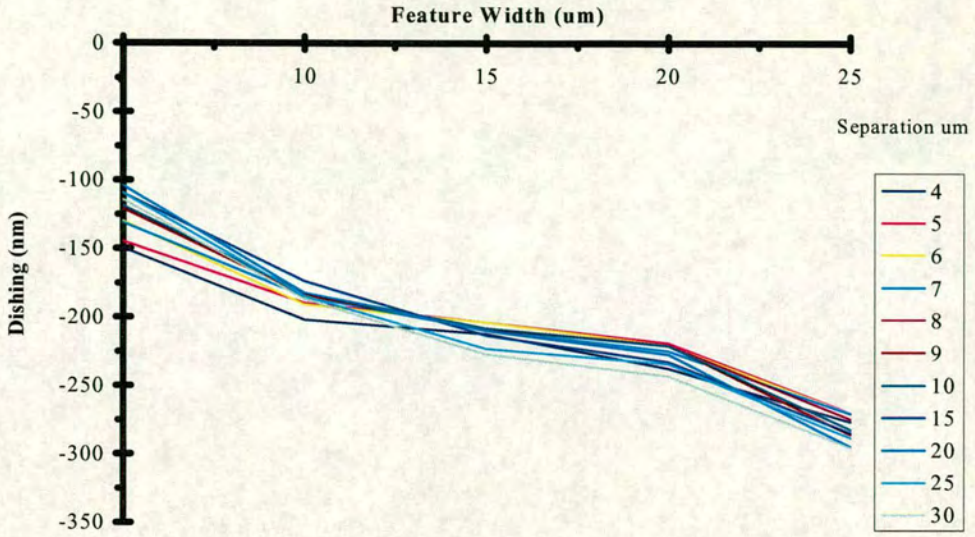


Figure 6.17 **Graph showing the degree of dishing against feature size (At different pattern densities)**

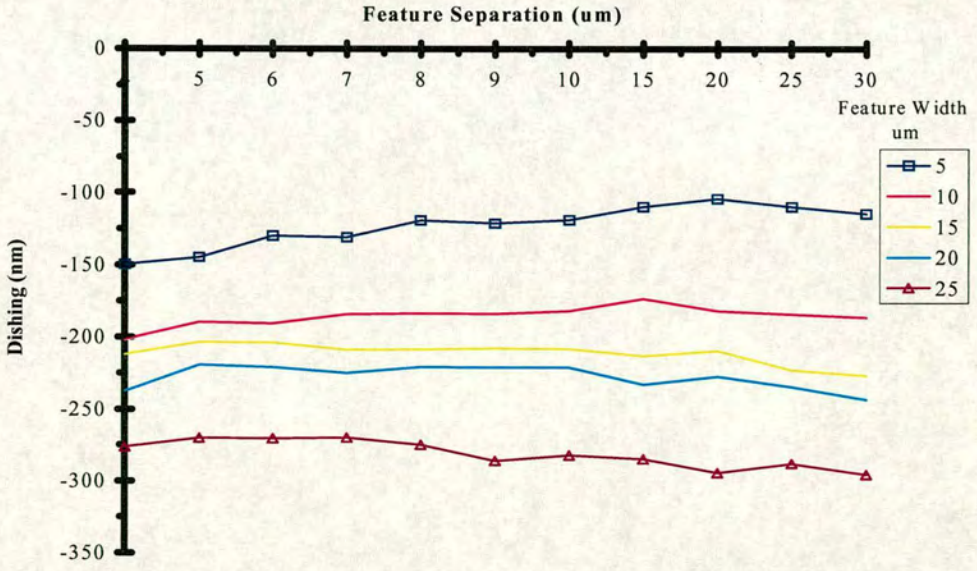


Figure 6.18 **Graph showing the degree of dishing as a function of feature density (For different feature widths)**

Figure 6.17 illustrates that the amount of dishing is a strong function of feature size. For a 5μm wide feature the amount of dishing is ≈140nm and for a feature 25μm wide it is ≈270nm regardless of spacing. As can be seen in Figure 6.18 dishing is only weakly dependent on feature density.

6.4.3. Erosion

Feature Width

The effect of feature size on erosion is shown in Figure 6.19. It can be seen that SiO_2 erosion is not a strong function of feature size. 10μm features spaced 5μm apart have 60nm of erosion, while 10μm features 20μm apart exhibit approximately the same level of erosion. As features become separated further the feature width starts to impact the amount of erosion induced. This is thought to be due to the effective length of the feature dense area. As the feature width increases, for the same feature spacing, it allows the pad to be deflected more easily as the "supporting" low feature density area is further away. Here again an analogy with a simple bending beam can be drawn.

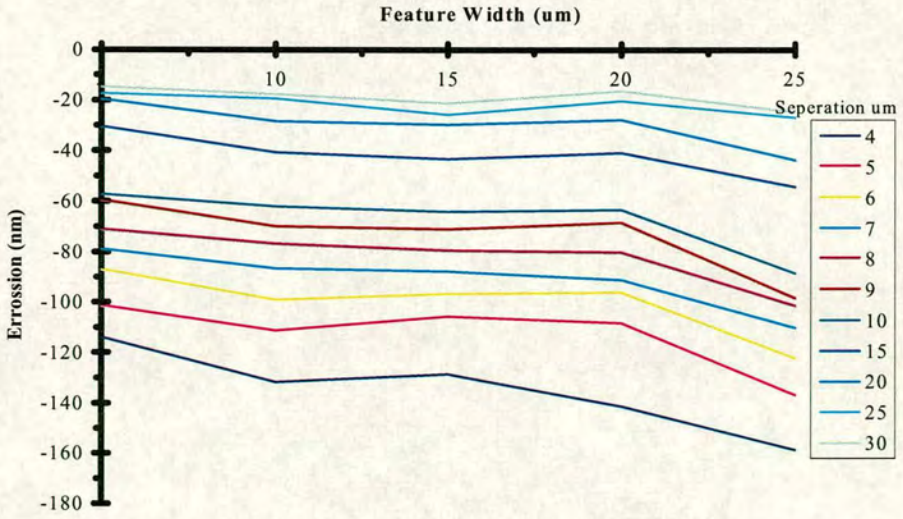


Figure 6.19 Graph showing degree of erosion as a function of feature width

Feature Density

Many authors Rutten *et al*[97], Chen *et al*[98] and Stine *et al*[99], among others, state that erosion is a direct function of pattern density. While this is undoubtedly true, other more subtle effects are also present. Figure 6.20 shows that at a given line width the closer together the features (higher the pattern density) the greater the degree of erosion. It clearly shows that there is a strong correlation between pattern density and erosion.

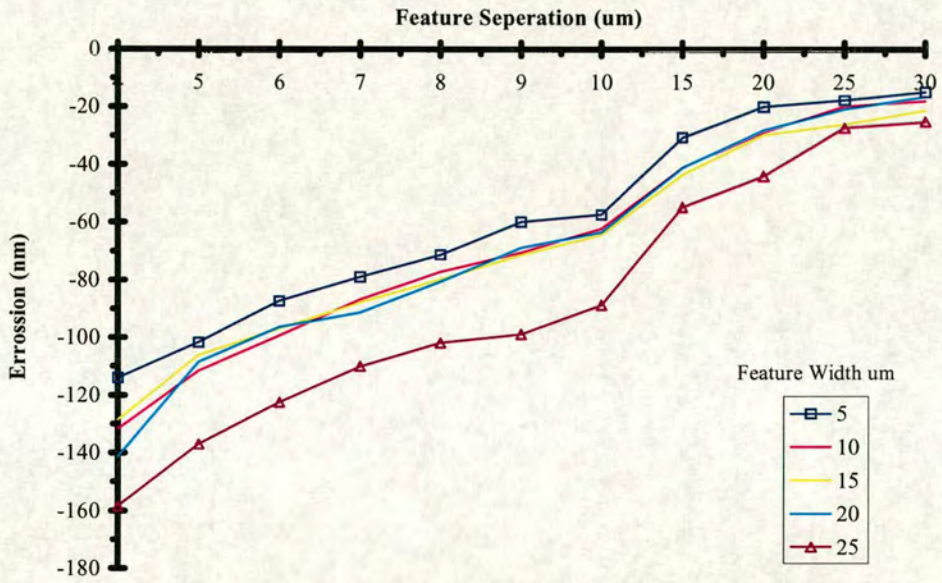


Figure 6.20 Graph showing amount of erosion against feature density

Investigating further indicates that this is a somewhat simplistic view. Within the test pattern are a number of line/spacing combinations which have identical pattern densities. Take, for example, equal feature/spacing regions, these have a pattern density of 50%. If erosion is a direct function of pattern density these should all exhibit the same degree of erosion. As can be seen in Figure 6.21 this is clearly not the case.

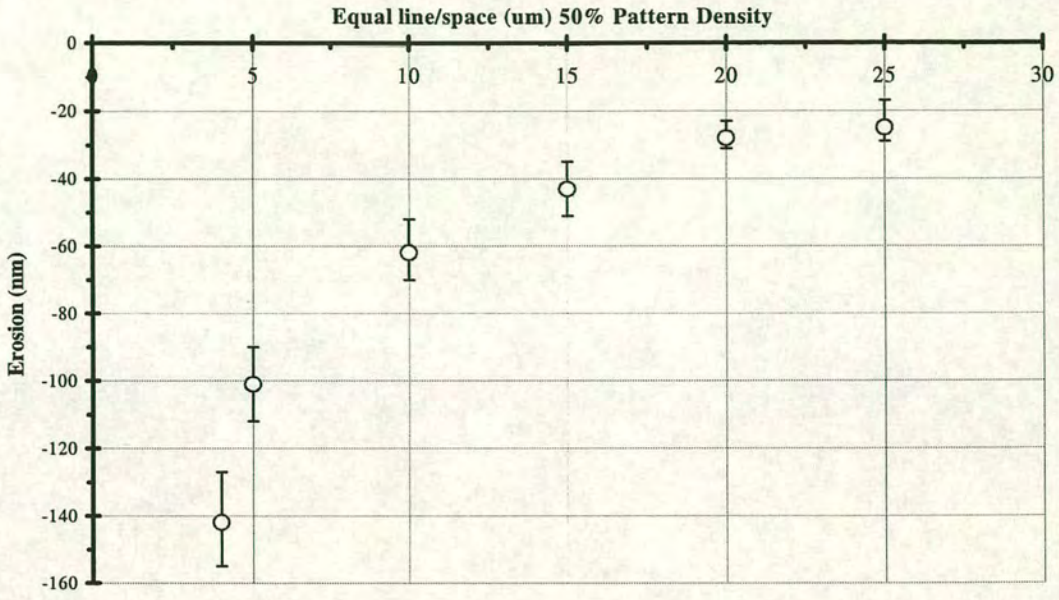


Figure 6.21 Graph showing the amount of erosion for "different" 50% pattern densities

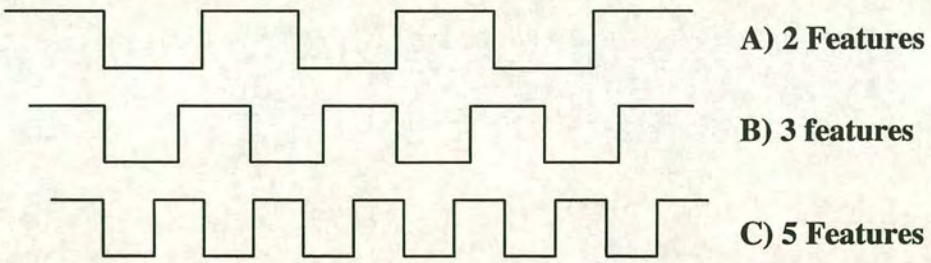


Figure 6.22 Diagram illustrating concept of different feature densities for the same pattern density of 50% (mark/space ratio)

As the line width shrinks so too does the SiO_2 'wall' separating them. These thin walls are more prone to erosion, leading to enhanced erosion at smaller feature geometry's compared to larger ones, for the same pattern density.

Another influence on erosion is the total area covered by a particular pattern density. Although the test pattern used did not have any structures of equal pattern density and of different size, it is thought that this will also effect the amount of dishing. An area of greater size than another, with equal pattern density, is expected to show more erosion. This can, again, be compared to the deflection of

a simple beam whose supports are moved further, apart therefore producing more deflection, Equation5.1.

6.5. Conclusion and Comments

It has been shown that while soft pads are less prone to cause scratching they induce undesirable amounts of feature dishing and SiO_2 erosion. They are therefore unsuitable for the planarisation of aluminium.

Hard pads, on the other hand, causes less although not zero amounts of dishing and erosion which, after some process optimisation may be able to be reduced further.

It has also been show that dishing is a strong function of feature size. The controlling factors governing erosion are far more complex; they depend on a range of variables including feature density, feature size and area of pattern extent.

The main findings are that erosion is not solely a function of pattern density. This is important when attempting to assess the amount of erosion which will be generated after polishing. It cannot be ascertained by simply determining the pattern density of a particular area. Areas with the same pattern density may polish differently and, conversely, areas with different pattern densities may polish in a similar fashion.

It was also found that wafer-scale polish uniformity plays a major role in almost every aspect of metal CMP. It increases the amount of dishing and erosion by making it is necessary to over-polish some areas to ensure the whole of the wafer is cleared. Altering the process variables (pressures and speeds) made little impact upon wafer scale uniformity, due to polishing in the fluid regime as opposed to the Hertzian indenter regime.

7. Mirror Damascene Introduction

The manufacture of SLMs using conventional techniques leaves the mirrors standing proud of the surrounding area by as much as 1.6μm, Figure 7.2, and with a poor surface smoothness, Figure 7.2*a*. This mirror thickness is necessary to ensure good via fill and hence a good electrical contact to the underlying circuitry

One problem with this method is that difficulties are created with LC filling, in the form of turbulence induced alignment defects caused by the LC flow[100] over and around the raised mirror elements[101], this phenomenon is termed capillary pinning[102]. This effect can be seen Figure 7.2*b*, in which the LC (Merck E7) fill is from left to right, with the cell gap set at 3.1μm using spacer balls mixed within the cover glass adhesive. As is observed the LC flow front is far removed from a linear shape.

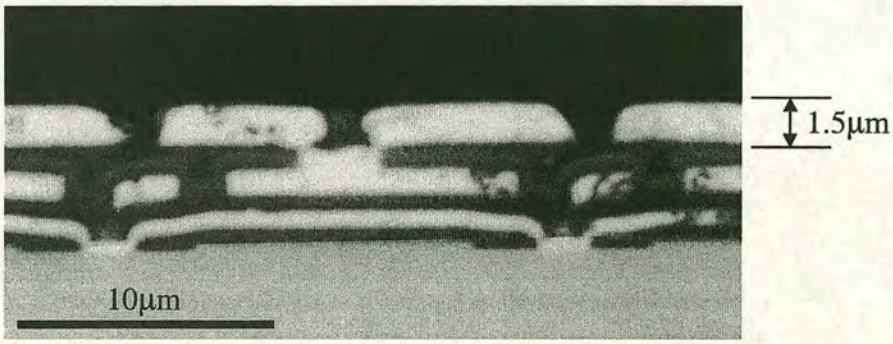


Figure 7.1 Crossection of a mirror and via of 512^2, device showing final mirror thickness

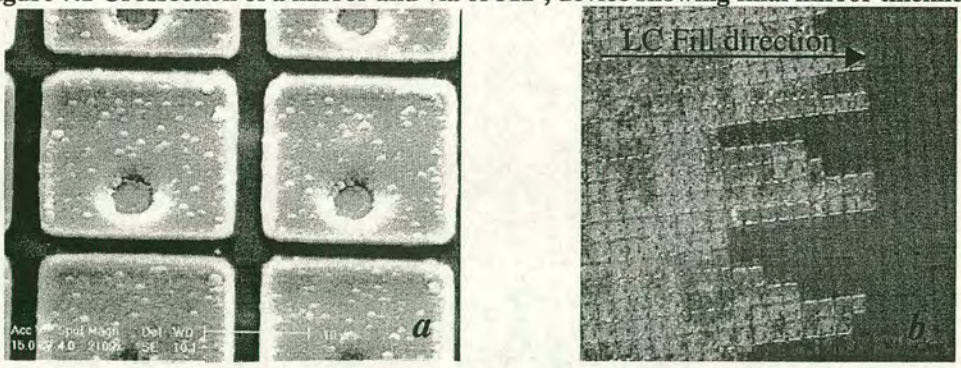


Figure 7.2 SEM of small part of 512 x 512 Display, *a*, and LC fill flow, *b*.

One way to overcome this problem is to manufacture mirrors whose surfaces are level with the dielectric insulating layer. O'Hara *et al*[103] suggested a dual damascene technique may be used for the manufacture of SLMs. In this chapter the work initially carried out by O'Hara is developed further and the problems raised will be investigated, and solutions sought.

The main problem with using this technique is their drive circuitry layout. It consists of a central feature dense area, the array, surrounded by feature sparse area, the field (Figure 7.7). This configuration is the root cause of many of the problems encountered while using the damascene method.

7.1. The Dual Damascene Process

The line first method (Appendix B), Figure 7.3, of dual damascene was used throughout the development process, in SLM devices the mirror is effectively the line. It was preferred over the via first method because it was thought it would be a more reliable because of the possibility of incompletely clearing the via of photo-resist during final mirror (line) patterning. This would leave resist in the via hole, therefore not allowing the it to be etched to its full depth and no contact being made to the circuitry below.

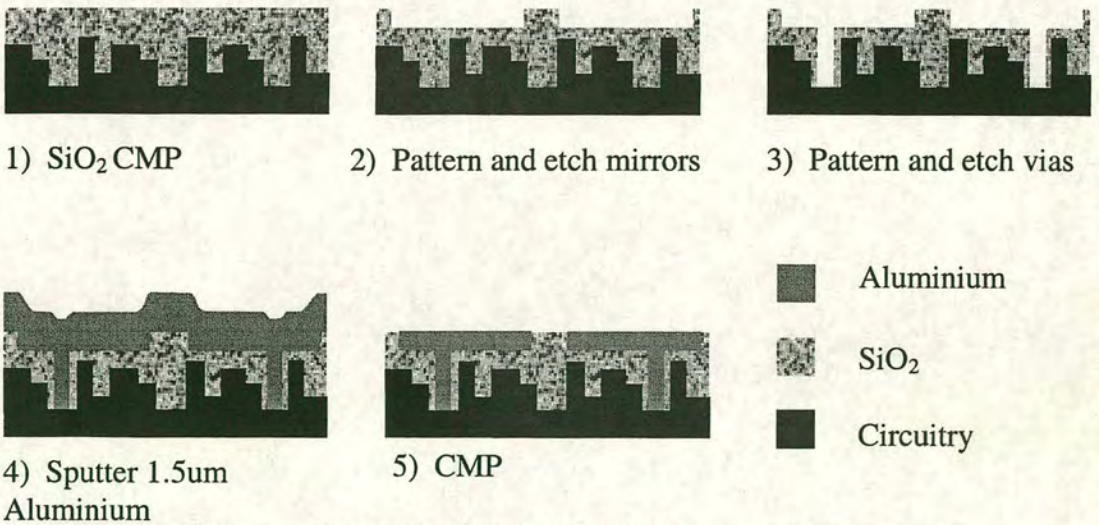


Figure 7.3 **Schematic of the line first dual damascene process.**

The absence of a hard stop layer necessitated that the mirror (line) depth was controlled by a timed etch cycle. The depth of the mirror (line) was half the total SiO_2 thickness, which in the case of the test wafers was 0.5μm with the via depth being etched to the same depth.

The use of CMP raises secondary concerns such as dishing of the individual features caused by differences in material characteristics between the dielectric and aluminium. Dielectric erosion, is another concern this is caused by the difference in pattern geometry on different areas of the die. Methods to minimise these will be investigated, and their effectiveness will be discussed.

Aluminium was chosen as the reflective material because of its high reflectivity (~92% at visible wavelengths) and compatibility with conventional microfabrication techniques. Unfortunately aluminium is relatively soft, with Brinell hardness of between 15 and 28 kg mm^{-2}, (compared with that for copper of 82 kg mm^{-2}) and therefore is easily scratched during polishing. Scratches are caused by a number of factors e.g. foreign particulates and abnormally large particles within the slurry. Metal slurries tend to age, in that the small sub-micron sized abrasives tend to agglomerate and form much larger particles, Figure 7.4*a*, sometimes tens of microns in size. Abraded material, thought to be aluminium oxide, which is not transported off the pad in the slurry and even the pad asperities themselves Figure 7.4*b*, are thought to contribute to scratching.

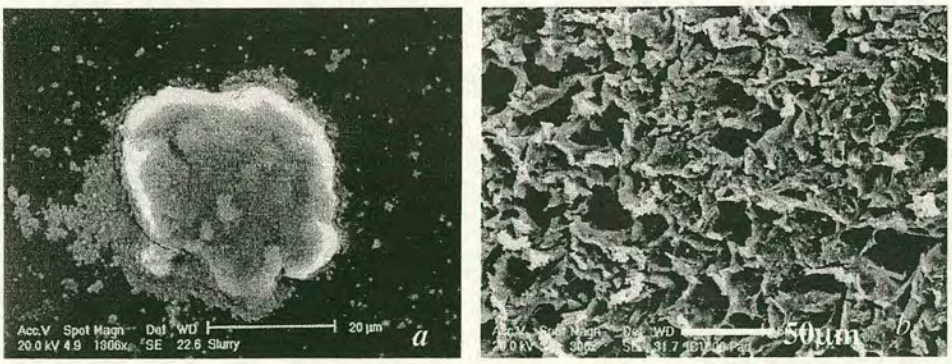


Figure 7.4 SEM of slurry particle caused by agglomeration (a SEM of surface of IC1000 CMP pad (b)

The surface roughness not only determines the reflectivity but also influences the LC fill dynamics, Figure 9.10. Cox *et al*[104] suggest that liquid flow characteristics are different for a rough and smooth surface. This may indicate that the presence of surface scratches could disrupt the LC flow front and therefore the final LC alignment quality. It is therefore essential that as good a surface finish as possible be achieved.

Figure 7.5 shows a case of severe scratching due to poor adhesion between the aluminium and the underlying dielectric. As the aluminium becomes thinner during polishing the large particulates within the slurry cause 'rip-outs', the resulting material can be very large in size causing the severe scratching observed. Note, also, the two parallel scratches running from bottom left to middle right. These are caused by either a large particulate becoming lodged within the pad or a pad asperity, which indicates that the pad may need to be conditioned.

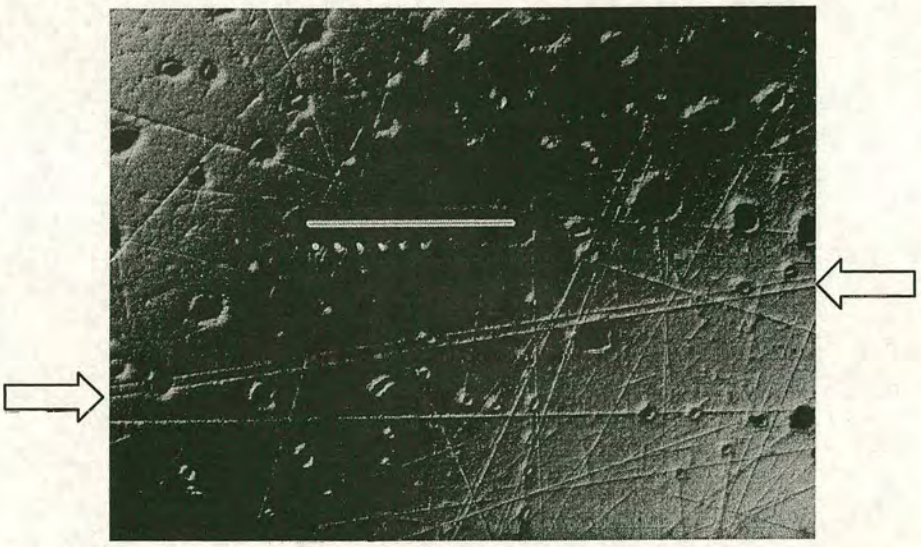


Figure 7.5 Photomicrograph of a severe case of scratching (The long thin feature is 10μm wide.)

The erosion of the dielectric within the array causes it to become a flat bottom 'bowl' shape. This is caused by aluminium in the high feature density region (array) clearing before the low-density (field) area, Figure 7.6. This exposes the inter-mirror dielectric 'walls' to the abrasive action of the pad/slurry. It takes a further two to three minutes for the low feature density area to become cleared of

aluminium. As this erosion will cause a variation in LC cell thickness it will have a detrimental effect on the LC fill dynamics. Mirror dishing is also introduced due to different material characteristics, which causes spurious colour fringes, due to different optical path lengths[105].

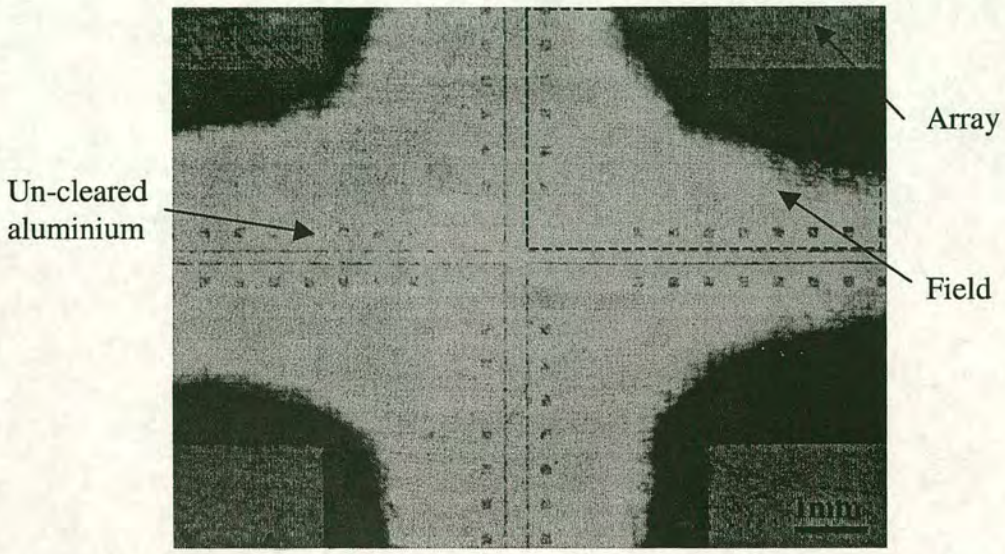


Figure 7.6 **Photograph of Part-polished wafer showing slow polishing of field area (The four rectangles, one in each corner, are the cleared arrays)**

A technique has been developed which helps to minimise the array erosion and mirror dishing problems. A block pattern is photo defined over the array region to leave the field region exposed. The aluminium in the field is then removed by wet etching, the resist is then stripped. This leaves aluminium in the array and bond pad regions only. It has two beneficial effects: the first is to reduce the overall polishing time; the second is to clear the zero feature density areas (the slowest to clear). This makes it possible to stop the polish when the array is clear, removing the necessity for further polishing to clear the field region.

7.2. Experimental Procedure

A damascene mirror photo-mask was produced by making a dark field copy of the original light field mirror mask. The layout, seen in Figure 7.7, was patterned into 1.0μm of ECR SiO_2 deposited onto 100mm diameter wafers.

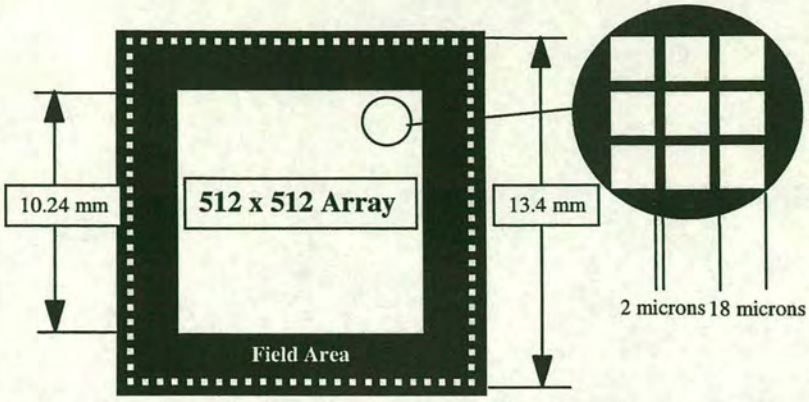


Figure 7.7 Dark field mask pattern used in mirror damascene tests

The oxide was etched to a depth of 0.5μm to create the mirror features, the vias were then photo-defined, using the original via mask, and etched to the same depth. The wafers were then sputter-coated with ~1.2μm of aluminium, a photomicrograph and surface profile of the pre-polished wafers can be seen in Figure 7.8.

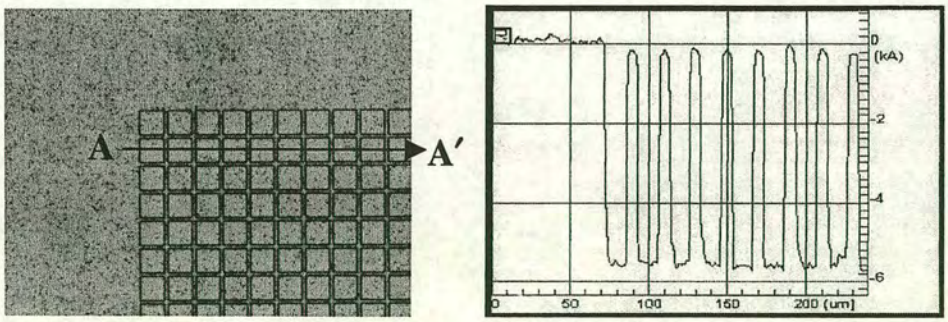


Figure 7.8 Photomicrograph showing corner of pixel array with its surface profile along AA′ to the right, before CMP

The polishing process was the same as previously described in Chapter 6 and is summarised again in Table 7-1. The pad conditioning regime was that developed in Chapter 6

Parameter	Setting
Pad	IC1400
Slurry	Rodel QCT1010
Oxidiser	15% H_2O_2
Slurry flow	200ml/min
Head speed	15 RPM
Table speed	10RPM
Head pressure	0.4 bar
Back pressure	0.3bar
Temperature	10°C

Table 7-1 Polishing parameters used in the mirror damascene tests.

The time to clear the wafer was approximately 15 minutes, giving a removal rate of 0.1μm/minute. After polishing the wafers were soaked in Ultracon detergent and then cleaned with a high-pressure water jet, and finally blown dry.

7.2.1. Results of Standard Mirror Damascene Technique

The final polished profile can be seen in Figure 7.9, which was taken using a white light interferometer. As the field of view was too small to obtain a full die image, data stitching was used. The die exhibits erosion of ≈0.3μm with dishing of ≈0.04μm, Figure 7.10. The gross curve in the image is due to wafer scale distortion and is not a product of the polishing process.

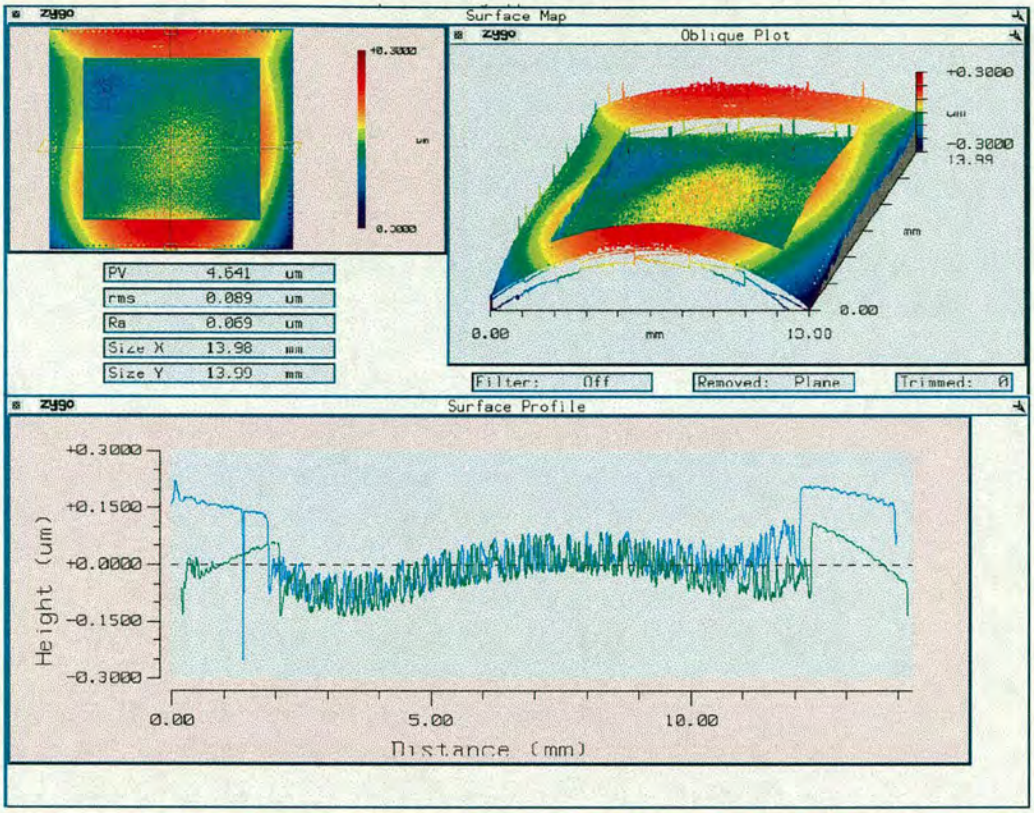


Figure 7.9 **White light interferometer image of pixel array, showing dielectric erosion in the array (~0.3µm erosion)**

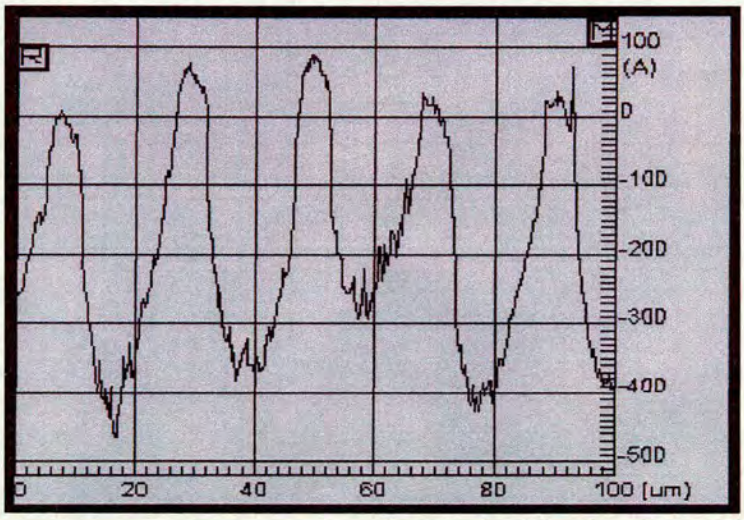


Figure 7.10 **Surface profile trace showing dishing of individual mirror elements with no pre-CMP etch with dishing of ≈0.04µm**

7.3. Pre-CMP Etch

As the level of erosion, using the standard dual damascene technique, was deemed to be too severe, a modified process was developed[106]. It consisted of a pre-CMP etch which was used to remove the aluminium from the slow-polishing field area. This was accomplished by photo-defining a resist 'block' mask over the array region, the bond pads were also patterned so as to leave the field area exposed, Figure 7.11. The aluminium was then removed using wet etching, and the resist removed before the wafers were polished.

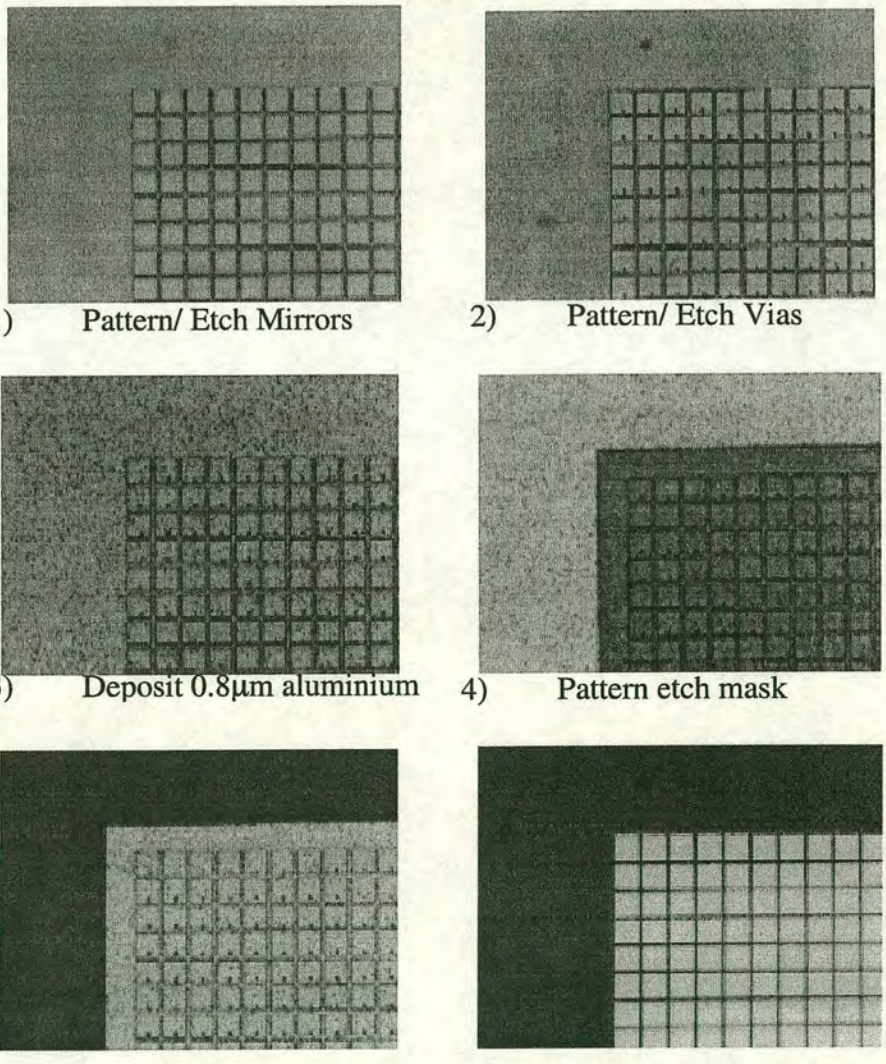


Figure 7.11 Process flow for pre–CMP etch

The final profile of the pre-etched wafer can be seen in Figure 7.12, this can be compared with Figure 7.8. It can be seen that the array is now ≈1.1μm higher than the field due to the aluminium being removed.

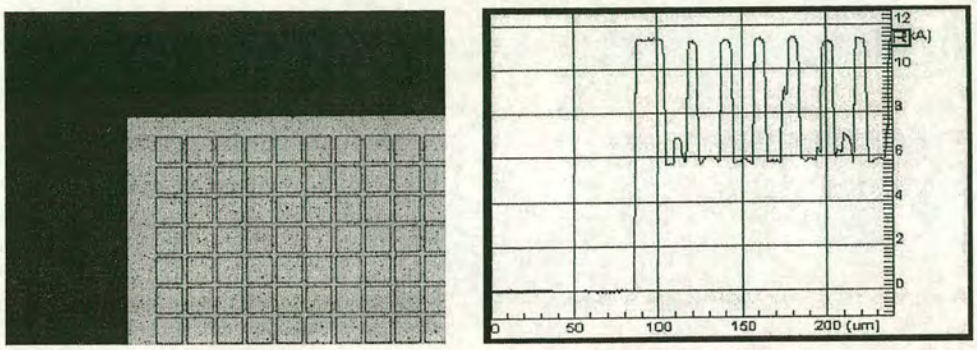


Figure 7.12 **Micrograph showing corner of array after etching with its surface profile to the right (pre-CMP etch)**

7.3.1. Results With Pre-Etch

The problem of wafer scale polish non-uniformity was again observed. The polishing of aluminium uses relatively low pressures, when compared to dielectric CMP. As such, the wafer warp plays a more prominent role in polishing uniformity. The warp can alter the ideal pressure distribution profile across the wafer, resulting in localised high pressure areas. As material removal rate is a function of pressure this in turn alters the removal rate, leading to anomalous removal patterns. This has the effect of causing more erosion, but little more dishing, in those areas that clear first. As each wafer has different warp characteristics this makes it difficult to predict the material removal pattern. The use of higher polishing pressure would help to alleviate this phenomenon but it was found to increase scratching and SiO_2 erosion, which was thought to be due to increased wafer/pad interactions.

7.3.2. Array Erosion in Pre-Etched Samples

The amount of erosion, with the pre-etched wafer, can be seen in Figure 7.13. The array has been eroded by ≈0.15μm. This is a result of the array being subject

to virtually zero overpolish time as the field area has already been etched clear. The amount of mirror dishing was unaffected and remained at ≈0.04µm.

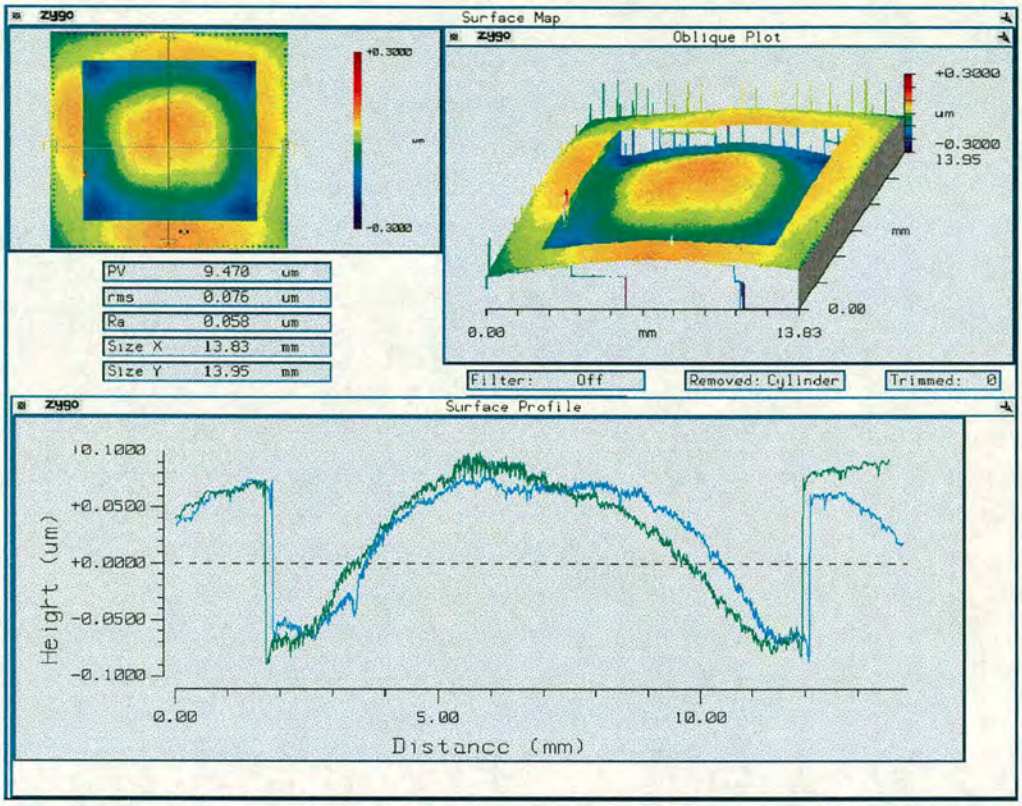


Figure 7.13 White light interferometer image showing pixel array showing 0.15µm erosion (with pre-CMP etch)

Although the overall erosion has been reduced by ≈50% the new profile is still far from ideal. This rounded array profile will have a detrimental effect on both the LC fill dynamics and on the optical quality of the device. This is caused by the aluminium 'mesa' over the array polishing edge-fast, Figure 7.14, this has the effect of exposing the inter-pixel walls at the edge of the array first. These are then over-polished before the centre of the array is cleared leading to the rounded array profile.

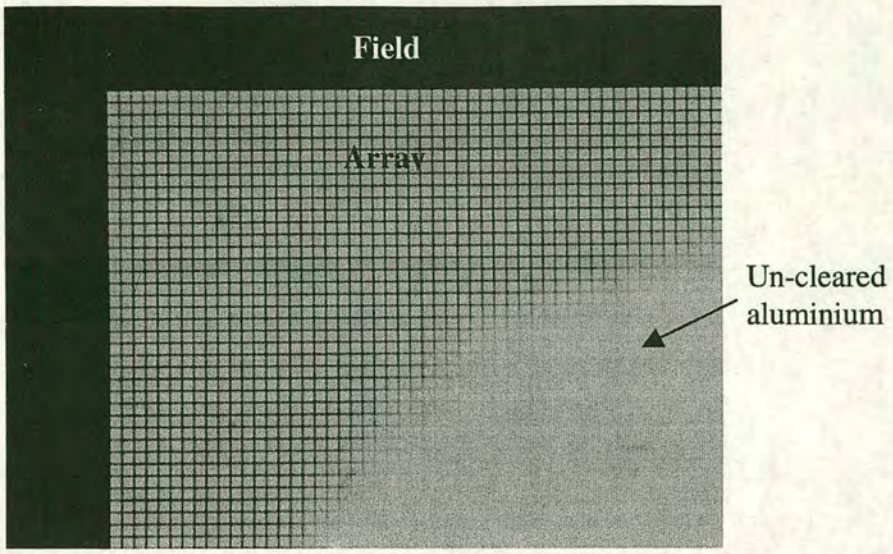


Figure 7.14 Photomicrograph showing corner of array clearing first (each pixel is 18 x 18 μm is size)

7.3.3. Pre-CMP Etch With 0.8μm Aluminium Step Height

The aluminium mesa has polishing in a similar way to the original SiO_2 step height of the pre-post-processed wafer. It was therefore concluded that by carefully selecting the pre-CMP aluminium step height the final array shape could be improved. Unfortunately in reducing the amount of aluminium deposited necessitates a reduction of the mirror and/or via etch depths. This was essential to ensure that the pre-CMP via surface still came above the SiO_2 layer so that no via dimple will be visible after polishing, Figure 7.15.

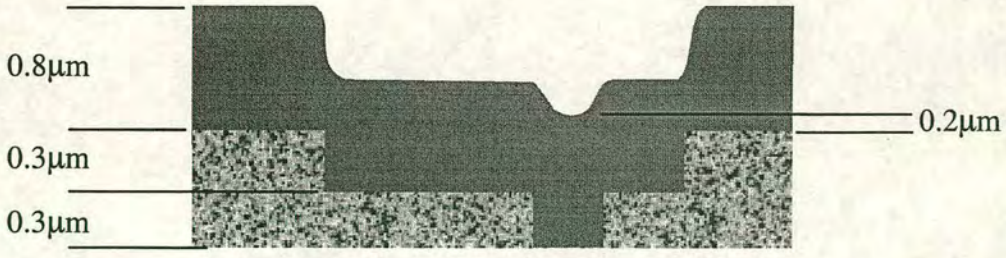


Figure 7.15 Schematic of via/mirror depth and aluminium fill height

To confirm this a test wafer was produced with mirror pits ≈0.3μm in depth, 0.8μm of aluminium was then sputtered deposited to create a 0.8μm step height, the surface profile of which can be seen in, Figure 7.16.

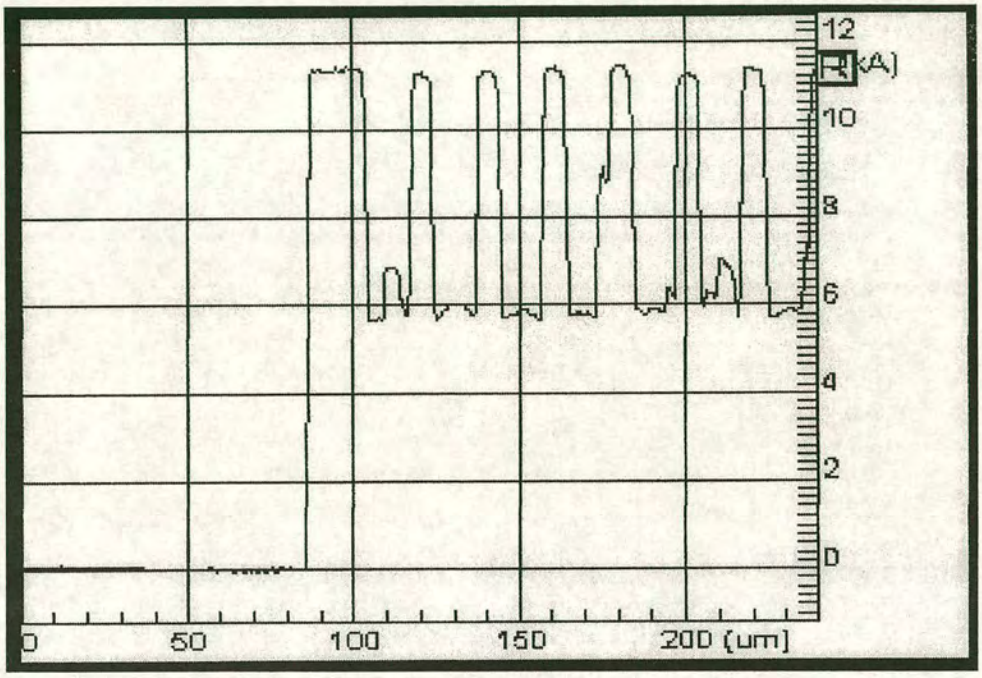


Figure 7.16 Surface profile of 0.8μm aluminium step height with pre-CMP etch

The resulting post-polish profile can be seen in Figure 7.17 and Figure 7.18. It can be seen that the profile is now far flatter with ≈0.07μm of erosion. The mirror dishing has also been reduced to 0.02μm. The edge effect, although reduced, is still present with a depth of 0.2μm and a width of ≈200μm. The die bow seen in the top right image is a function of wafer bow and is not a product of the aluminium polishing process.

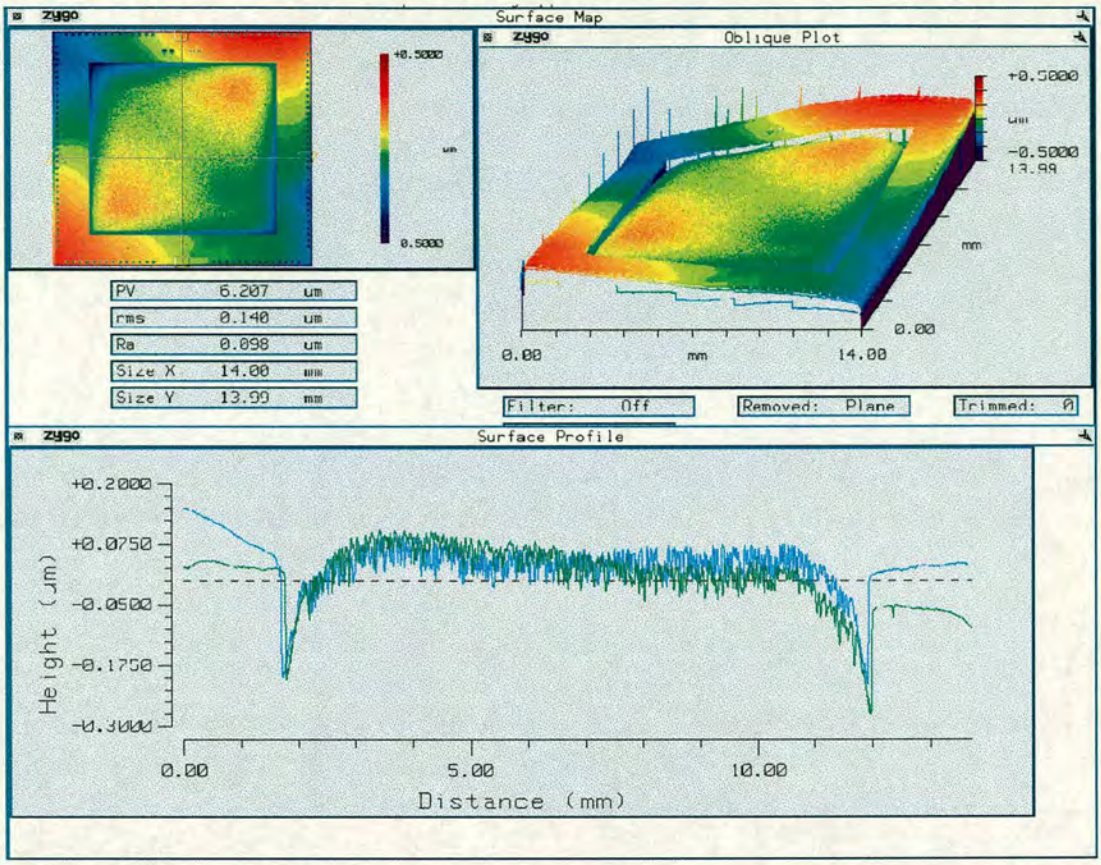


Figure 7.17 **White light interferometer image showing array erosion in a pre-etched wafer with 0.8µm aluminium step height**

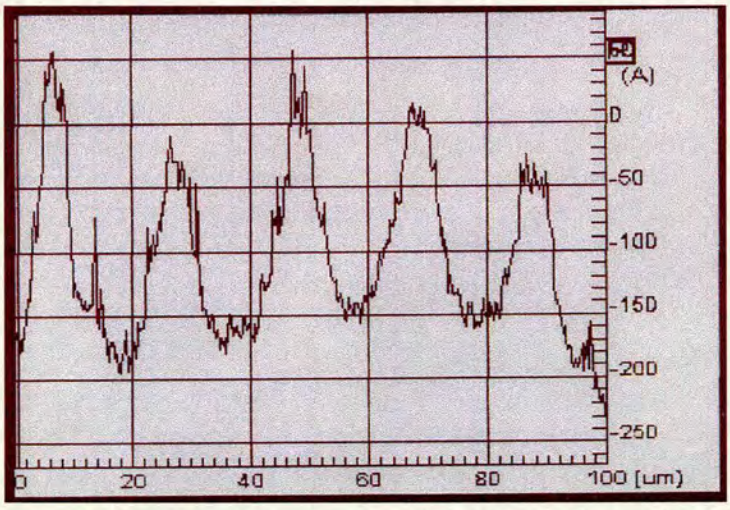


Figure 7.18 **Surface profile trace showing dishing of individual mirror elements with pre-CMP etch wafer with 0.8µm step height with dishing of ≈0.02µm**

An SEM image of the damascened mirrors using 0.8µm aluminium step height can be seen in Figure 7.19*a*. When compared to the original mirror quality (Figure

7.2*a*) several improvements can be seen. There is an improvement in the surface roughness, also the via 'dimple' is no longer present. The lack of via dimple will increase the fill factor from 80% to 84%.

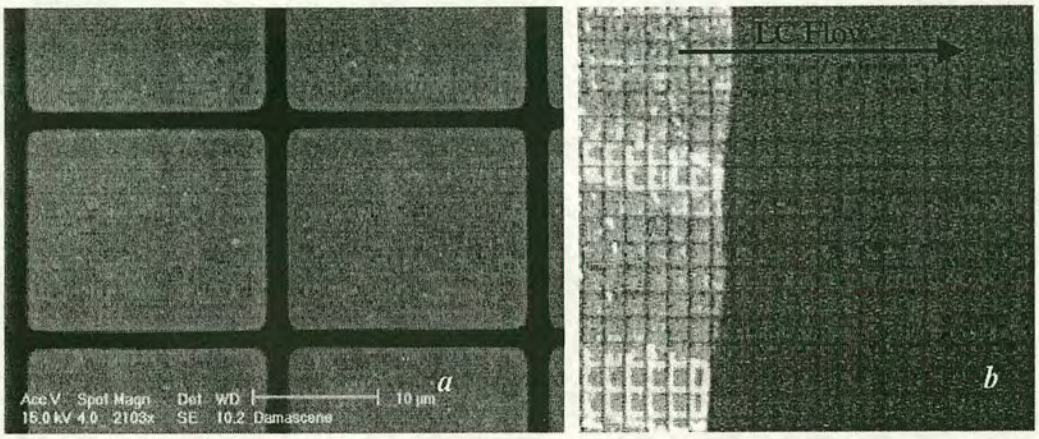


Figure 7.19 SEM of Damascened mirrors, *a*, and photomicrograph of greatly improved LC flow front, *b*

7.4. Conclusion and Comments

The use of a dual damascene technique to produce mirrors, which are level with the dielectric surface, has been investigated. Although the process removed the large mirror step height produced when using traditional fabrication methods it introduced new problems. These included array erosion, mirror dishing and scratching. By far the biggest concern was the amount of array erosion as this would cause LC fill problems and interference fringes in the finished display due to different LC thickness. To over come some of these problems a novel pre-CMP etch technique has been developed.

The use of a pre-CMP etch to remove the slow polishing aluminium in the field area reduced the array erosion from 0.3µm to 0.15µm. The amount of dishing was, however, unchanged. It was seen, that this reduction in erosion was accompanied by far from ideal array profile. The use of a carefully selected aluminium deposition thickness, combined with the pre-CMP etch, resulted in array erosion of ≈0.07µm and dishing of 0.02µm. The mirror surface roughness was also improved with the original mirrors having a RMS of 35nm and the dual

damascened mirrors having an RMS of 17nm. This will lead to improvements in reflectivity and LC flow over the mirror itself. The lack of the via dimple will also improve the local LC flow pattern, but it has the added advantage of increasing the mirrors 'useable' area, thereby increasing optical efficiency of the device.

A possible method to remove the problem of the edge groove is the use of sacrificial pixels around the edge of the array[107]. These pixels approximately 10 rows, or 200μm, in width would still be eroded but as they are not part of the active array area their erosion would not cause degradation in optical quality at the edge of the array.

8. Via Damascene

It has been shown that the use of dual (mirror) damascene removes the mirror step height but induces new concerns such as array erosion and mirror dishing. Another method to decrease the mirror step height, and improve the surface quality of the mirrors, is by the use of 'thin' mirrors (deposited on a planarised SiO_2 surface). These are mirrors whose thickness is $\approx$0.1μm instead of the conventional 1.5μm. The reduction in mirror thickness also improves the surface quality (see Chapter 9).

The use of CMP to produce vias, which are level with the dielectric surface, is a critical step in the manufacture of thin mirror devices. Producing vias which are level with the surface of the insulating dielectric allows for the deposition of a thin metal mirror layer. In the standard process the top metal has to be thick enough to ensure adequate step coverage[108], and therefore contact with the underlying circuitry. As the SiO_2 is $\approx$ 1μm thick a metal thickness of $\approx$1.5μm needs to be deposited, Figure 8.1. This thick aluminium has several drawbacks:

1 The surface quality, and hence the reflectivity, is poor (Figure 1.12*a*)

2 The large via dimple leads to a loss in fill factor

3 The large mirror step height which perturbs the LC flow front leading to poor final alignment (Figure 1.12*b*)

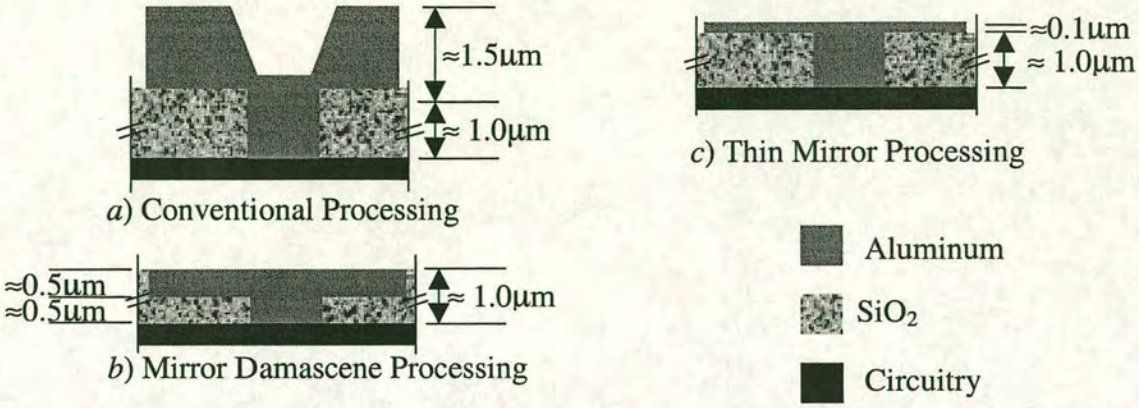


Figure 8.1 Comparison of conventional, dual damascene and thin mirror structures

To overcome these problems the vias are polished level with the surface of the SiO_2 using a metal damascene technique. This removes any step coverage concerns and so allows the deposition of a thin, ≈0.1µm, mirror metal.

To ensure the reliability of this technique several questions had first to be answered:

1 The amount of via dishing induced by the polishing process

2 What are the electrical characteristics of the polished via

3 What is the condition of the SiO_2 surface after polishing

The amount of dishing will affect how much metal has to be deposited to ensure good electrical contact with the via, it will also have a secondary optical effect. If the dishing is large it will introduce spurious optical signals into the reflected light.

Metal CMP works by forming a chemically induced oxide on the surface to be polished and then physically abrading it, Chapter 7. This oxide, thought to be Al_2O_3 for aluminum, is an insulator and as such needs to be removed before the top level metal can be deposited. As the Al_2O_3 is chemically induced it will be thicker than the native oxide, of ≈4nm[109], which is always present on the surface of the aluminium.

The condition of the SiO_2 surface post via damascene will affect the quality of the mirrors. If the surface is severely scratched the final metal being thin (≈100nm) will conform to this and so will be degraded.

To answer these questions a test structure was designed and manufactured. The layout of which can be seen in Figure 8.2, and a schematic cross section can be seen in Figure 8.3

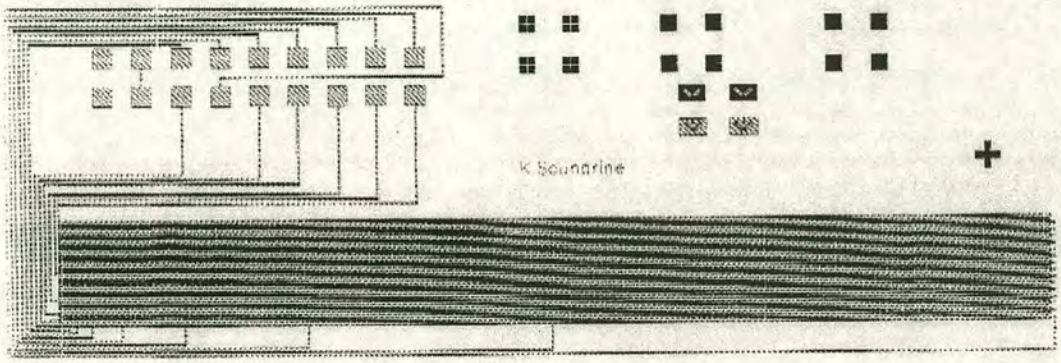


Figure 8.2 Cadence layout of via test pattern (Designed in conjunction with K. Seunarine)

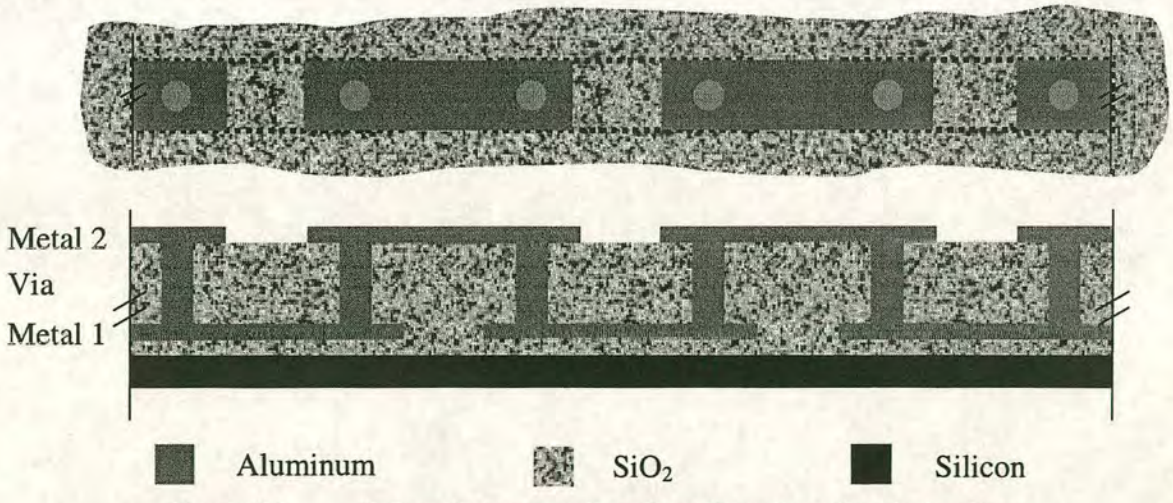


Figure 8.3 Schematic cross-section of small portion of via test pattern

The test pattern consisted of a serpentine containing 4096 vias with tap-offs at 2, 4, 8, 16, 32, 64,128, 256, 512, 1024, 2048 and 4096. The via diameter was 2μm and placed on a 20μm pitch i.e. the same as the product 512^2 SLM. This enabled the investigation of the via contact resistance for different numbers of

interconnects, on the same test design which were arranged in a four terminal Kelvin layout[110].

8.1. Fabrication of Via Test Structure

The fabrication steps of the test structure can be seen in Figure 8.4. It was patterned onto 100mm wafers, which had previously been oxidised to insulate metal 1 from the silicon substrate. The aim was to create a structure that would allow the replication of the process steps necessary to polish the vias on a product wafer. The inter-metal dielectric, SiO_2, was polished using the same process and to the same thickness (≈1.0μm) as it would be on a product wafer, Chapter 4

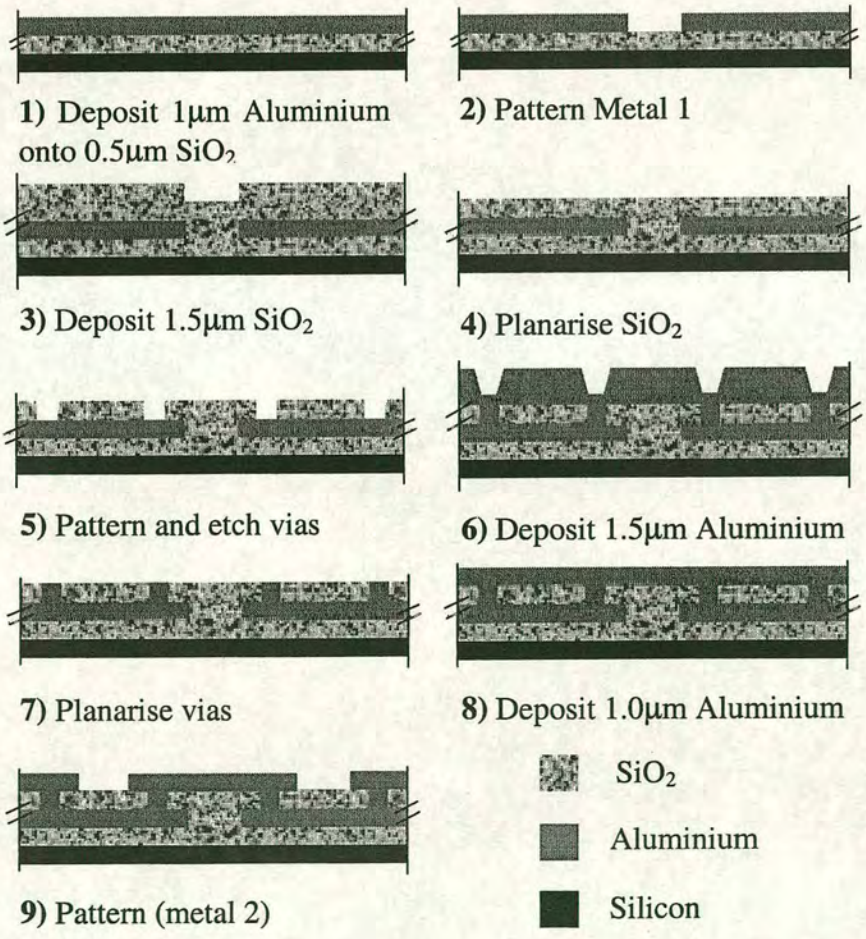


Figure 8.4 **Process steps for the manufacture of the via chain resistance test structure**

8.2. Via Filling

Before the via level metal is deposited a sputter clean has to be performed, Figure 8.5. It consists of bombarding the wafer with accelerated argon atoms, which has the effect of removing surface material by a sputtering action. This is to remove the native Al_2O_3 which would cause a high resistance between the bottom of the via and the contact metal.

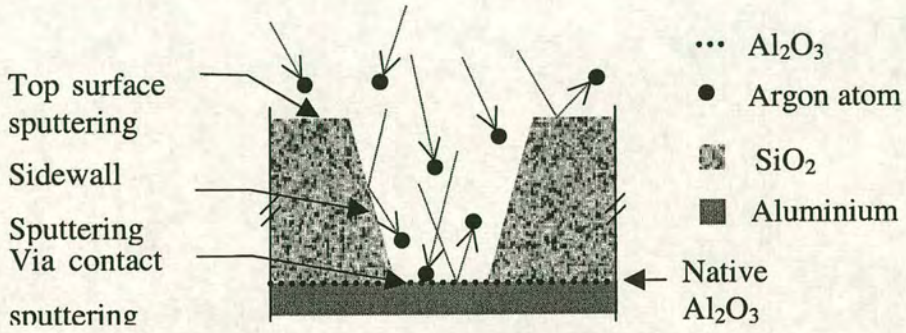


Figure 8.5 Schematic illustration of the sputter cleaning of bottom via contact

At this stage it is important not to expose the wafer to excessive sputter cleaning. The argon atoms not only sputter the Al_2O_3 at the bottom of the via hole, but also the sidewalls themselves. This can lead to sputtered SiO_2 (from the sidewalls) being deposited onto the contact area[111]. This may cause a high contact resistance where the aim is to ensure a low contact resistance between metal 1 and the via. Once the clean has been performed the aluminium can be deposited without breaking the vacuum on the chamber.

An important consideration when using damascened vias is to ensure that the via is completely full of metal and no voids[112] have been introduced during deposition, Figure 8.6

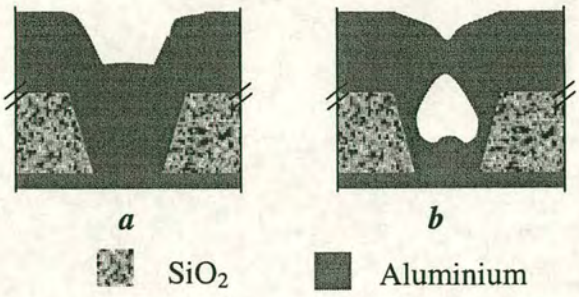


Figure 8.6 **Different via fill profiles *a)* ideal via damascene fill (via completely full of metal) *b)* 'Key hole' void**

With conventional processing the metal does not have to completely fill the via. The only criteria is for good electrical contact to be made with the underlying circuitry. When the via is to be subject to CMP it has to be completely full. This then enables the overburden to be removed by CMP leaving a via whose surface is planar with the surrounding dielectric. One problem is the possible non-complete filling of the via, these voids or 'key holes' are exposed after polishing. Although adequate electrical contact can be made the void tends to fill with polishing debris which is difficult (if not impossible) to remove This can then lead to reliability issues in the finished device. The void also leads to a reduction in the effective cross-sectional area of the via, creating current 'hot spots' which may cause electromigration[113].

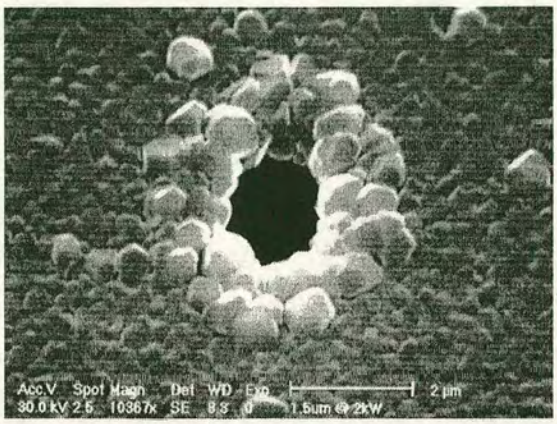
8.2.1. Via Filling Tests

In order to investigate the via fill properties of the Balzers sputterer several test samples were filled at different deposition rates. The test samples consisted of the 512^2 via pattern etched into 1μm of ECR oxide. Then 1.5μm aluminium was deposited at different rates to observe the effect on via fill properties. The parameters can be seen in Table 8-1 (all other parameters were kept constant). SEM images of the filled vias can be seen in Figure 8.7.

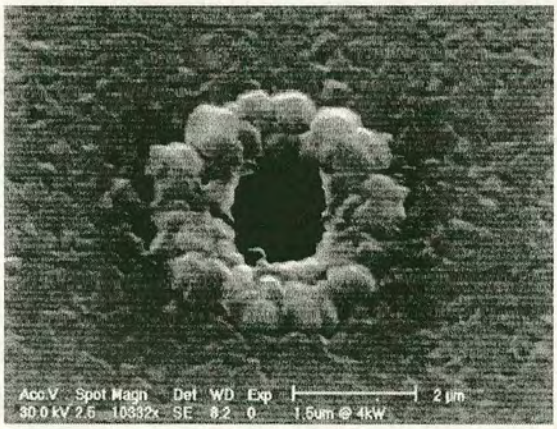
Sample Number	Deposition Power	Deposition Rate
1	2 kW	0.3 μm/min
2	4 kW	0.6 μm/min
3	6 kW	0.9 μm/min

Table 8-1 Deposition parameters used in via fill tests

1) SEM of via at 2kW



2) SEM of via at 4kW



3) SEM of via at 6kW

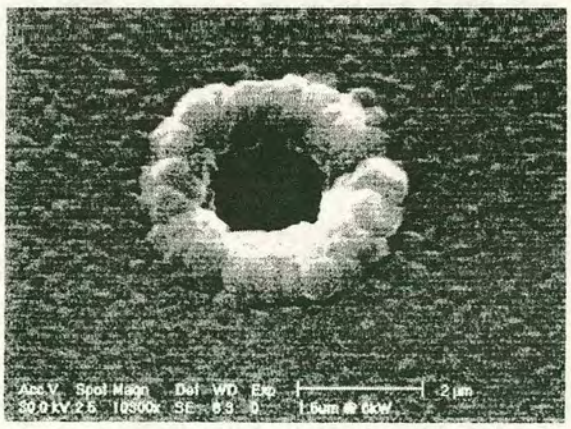


Figure 8.7 SEM images of 2μm vias filled at different aluminium deposition rates

8.2.2. Via Fill Observations

From Figure 8.7 it can be observed that sputtering aluminium at higher power produces a more open via hole. This indicates that there is less likelihood of creating keyhole voids within the deposited material. Although the surface of the aluminium finish becomes rougher at higher deposition temperatures this is not an issue. This is because the aluminium overburden is removed after polishing and the final, thinner, mirror metal deposited at low power.

8.3. The Via Damascene Process

The blanket-coated wafers are then subjected to CMP. The same conditions as used for dual damascene were used, Table 8-2 The result can be seen in Figure 8.8, the vias are just visible as bright dots at the ends of each metal 1 track.

After polishing, the wafers were cleaned in detergent, rinsed in DI water and spun dried.

Parameter	Setting
Head Speed	15 RPM
Platen Speed	10 RPM
Head Pressure	0.4 bar
Back Pressure	0.2 bar
Temperature	10°C
Pad	Rodel IC1400
Slurry	Rodel QCT1010
Oxidiser	15% H_2O_2

Table 8-2 Process variables and consumables set used in via polish tests

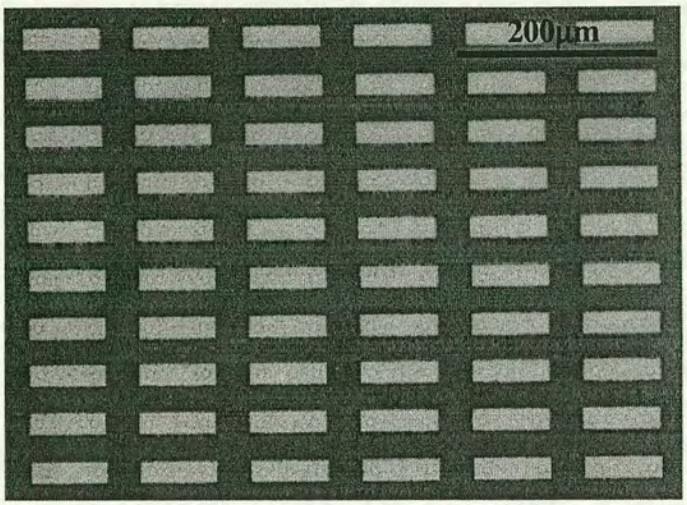


Figure 8.8 **Optical micrograph showing test structure after via damascene**

8.4. Top Metal Deposition

The critical process step is step 8 in Figure 8.4, the deposition of metal 2. The correct pre-metal 2 deposition sputter clean time had to be determined to ensure all the CMP induced contamination is removed from the via surface Figure 8.9. To investigate this, several sputter clean times were selected 0, 5, 7.5, 10, 15 and 20 minutes. As samples were in short supply a mask was made which had an aperture of ¼ of a wafer. In this way each wafer could be exposed to 4 different sputter clean times, making it possible to carry out all tests using two 100mm wafers.

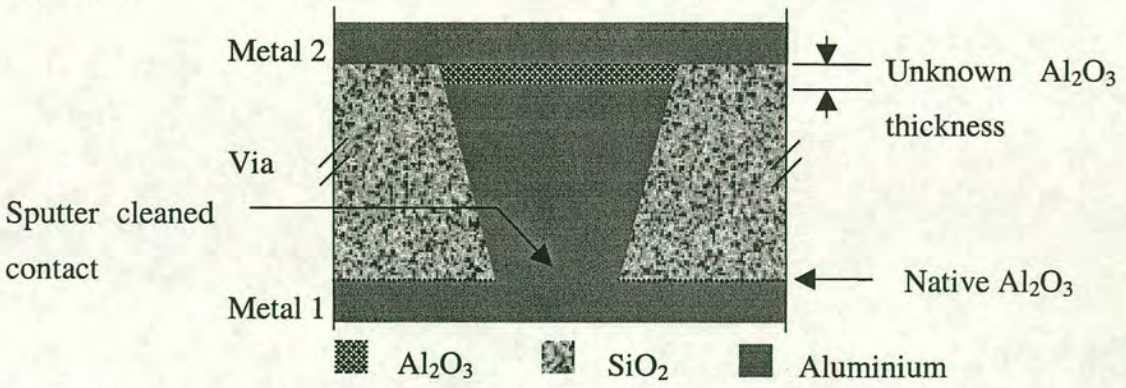


Figure 8.9 **Schematic cross section of a post-CMP via showing unknown Al_2O_3 thickness layer**

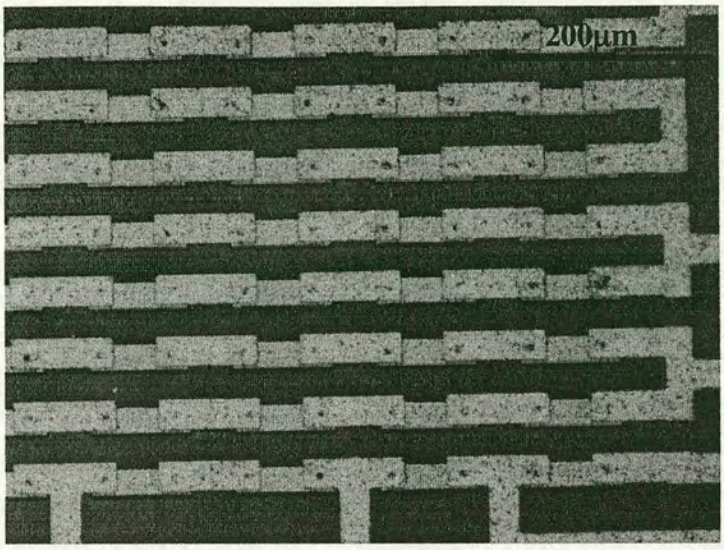


Figure 8.10 Photomicrograph Showing a corner of the finished test structure (Note: metal 2 is slightly misaligned, with respect to metal 1, but still makes good contact with the vias)

8.5. Results

8.5.1. Via Dishing

The amount of via dishing had to be ascertained to ensure that the process variables selected were correct. To do this a polished wafer was investigated using an AFM. The resulting images can be seen in, Figure 8.11 Figure 8.12. Several interesting points can be observed in the AFM images. The via at the center of the wafer, Figure 8.11, shows signs of dishing in the order of 48nm with the surrounding oxide showing slight signs of scratching. When compared with a via located at the edge of the wafer, Figure 8.12, the amount of dishing is comparable, 50.7nm, but there is substantially more scratching and surface damage surrounding the via.

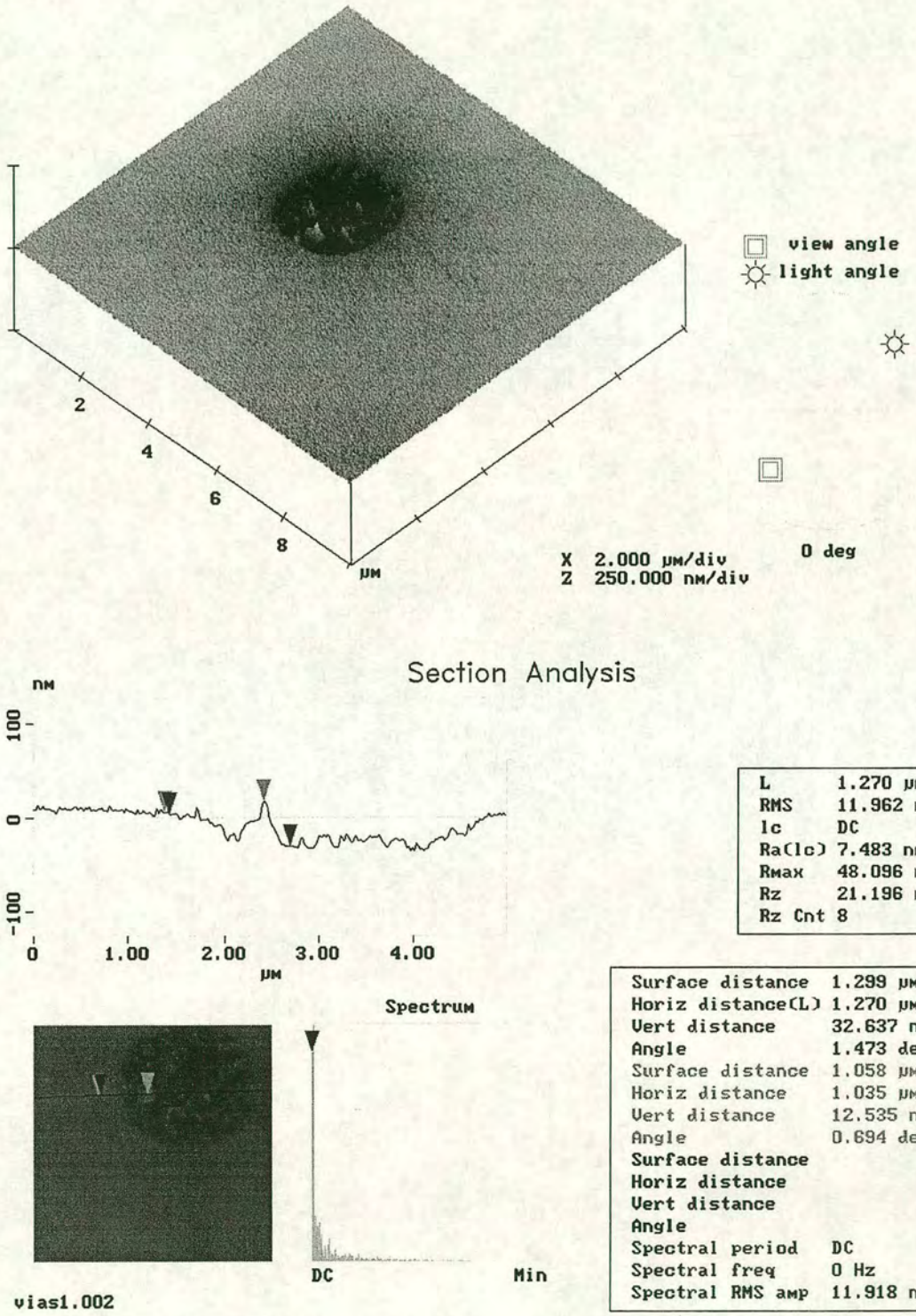


Figure 8.11 **AFM image and cross-section of a via in the center of the wafer**

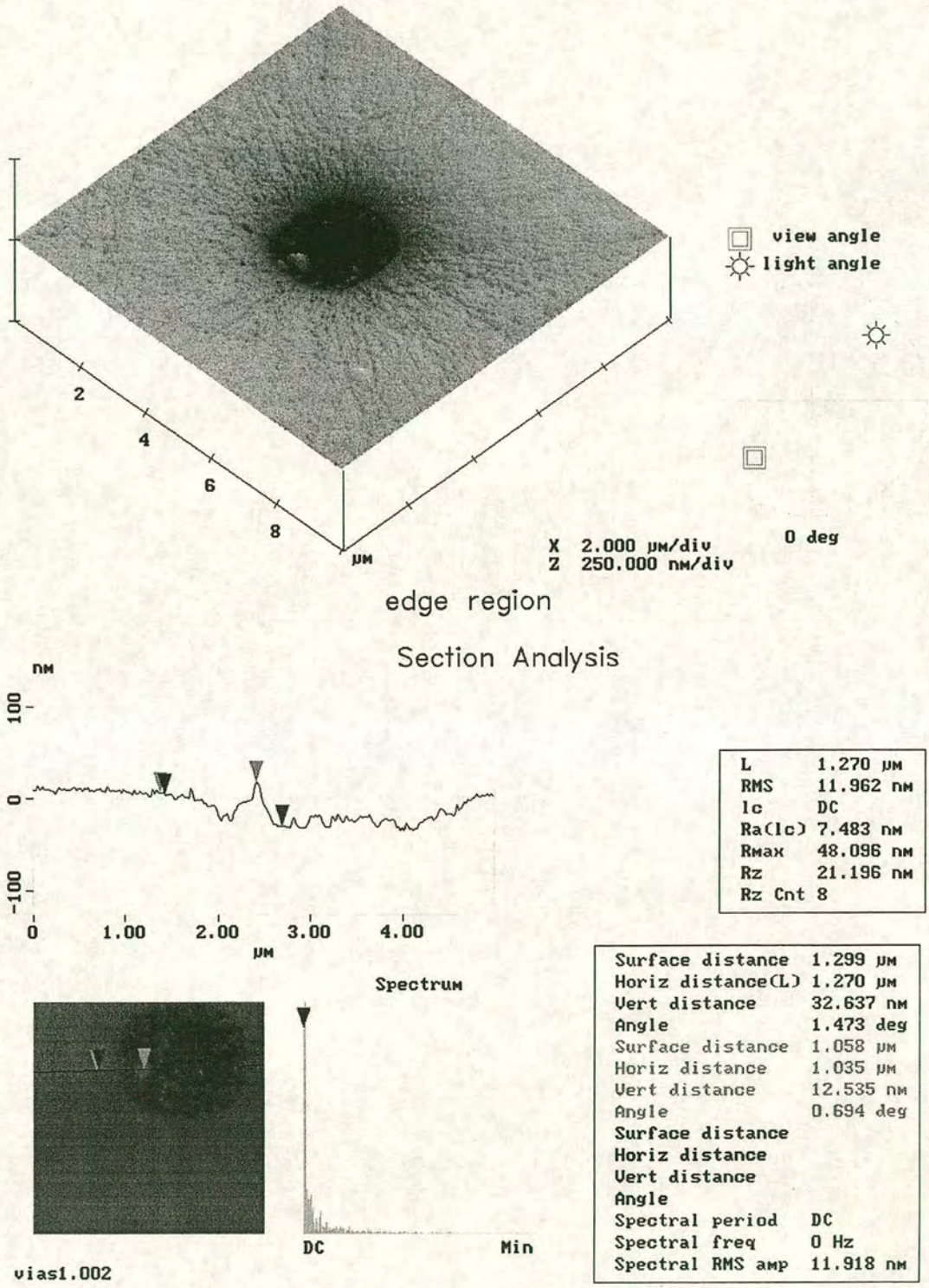


Figure 8.12 AFM image and cross-section of a via at the edge of the wafer

The cause of the severe scratching at the edge of the wafer (Figure 8.12) is due to the poor wafer scale polish uniformity, which was also seen in the dual damascene wafers. The edge of the wafer clears of aluminium first so exposing the underlying SiO_2. This is then eroded away, but as the dishing is a function of feature size, little more dishing is induced. As with the mirror damascene wafers the head pressure is low so the intrinsic wafer bow plays a greater role in the wafer scale uniformity.

Although the feature density is considerably less than that of the mirror pattern (dual damascene) the array area still cleared of aluminium before the field region. It resulted in some vias being subject to an inherent over-polish time. The amount of over-polish time was greater at the edge of the wafer due to the non-uniform wafer scale polish. This contributed slightly to the via dishing but more significantly to the via edge erosion and dielectric surface degradation.

It was found that 'double' printing of the mirror pattern and then removal of the field aluminium (as for the mirror damascene method) by wet etching, Figure 8.13, considerably reduced the polish time. Double printing consists of moving the wafer/mask alignment between the two exposures thereby producing smaller mirrors and less metal to remove by polishing. The polishing time of a blanket wafer with 1.5μm of aluminium was ≈15 minutes (≈100nm per minute). The time taken to polish the pre-etched wafer was ≈4 minutes. This reduction in polish time reduced the amount of edge to center erosion variation but did not significantly alter the amount of dishing observed.

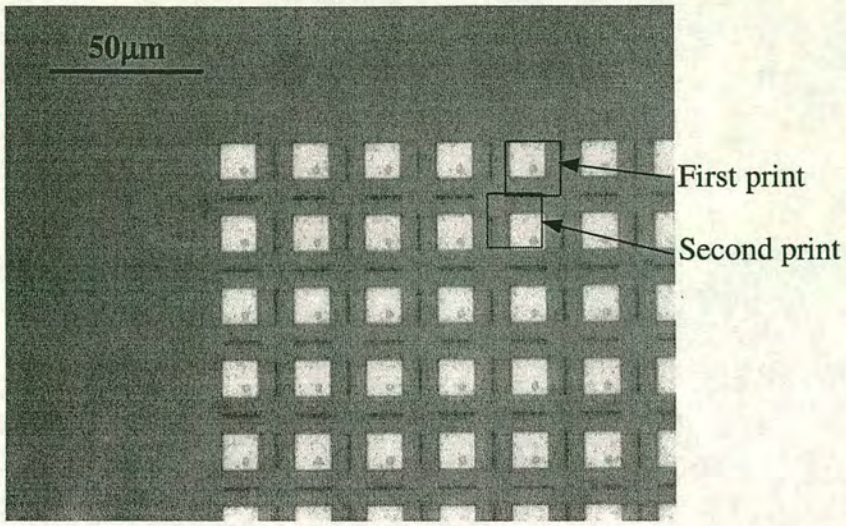


Figure 8.13 **Photomicrograph of pre-etched via array pre-damascene**
Note the double mirror photo pattern

8.6. Post Metal CMP Oxide Buff

Although the use of the pre-CMP metal etch produced a more uniform polish across the wafer it did not remove the CMP induced damage to the SiO_2. This damage, scratching as well as erosion would produce a degraded mirror surface. The use of a post-metal CMP SiO_2 buff was investigated for its effect on both the SiO_2 surface and via dishing. The parameters used for the buff are summarised in Table 8-3

Parameter	Setting
Head Speed	30 RPM
Platen Speed	30 RPM
Head Pressure	0.5 bar
Back Pressure	0.15 bar
Temperature	10°C
Pad	Rodel IC1400
Slurry	Klebosol 30H50

Table 8-3 **Process variables and consumables set used in via SiO_2 buff**

The buff was carried out on samples which had no pre-CMP metal etch and the results can be seen in Figure 8.14; the total amount of SiO_2 removed was ≈0.1µm.

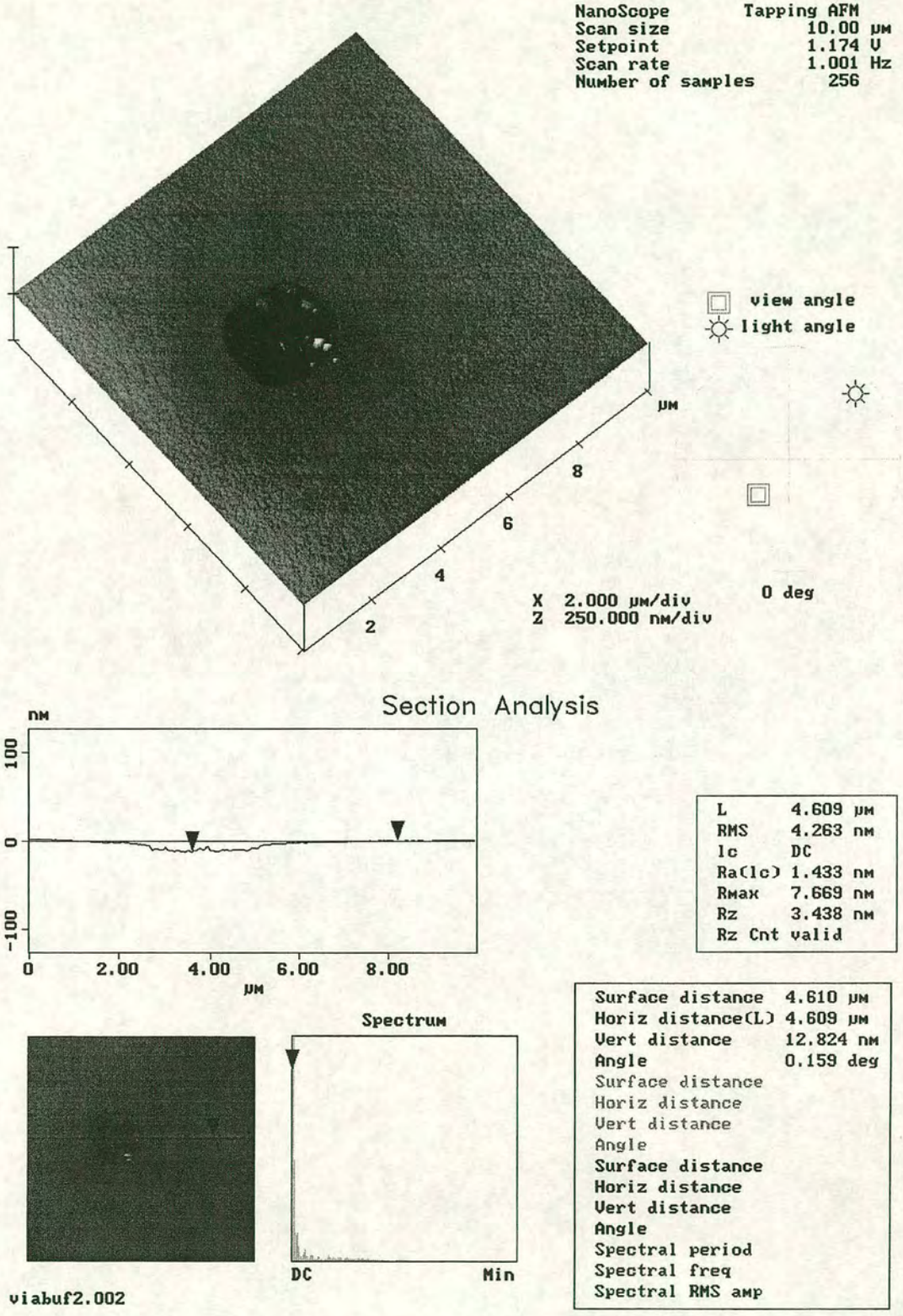


Figure 8.14 **AFM image and cross-section of a via after 2 minutes oxide 'buff'**

Several improvements are clearly seen in Figure 8.14 when compared with Figure 8.11. The first is the total elimination of any SiO_2 scratching and erosion. The surface finish of the SiO_2 surrounding the via is the same as that found on blanket SiO_2polished wafers, ≈0.2nm RMS. The second is the reduction of dishing from 50nm to 14nm. Another improvement is the wafer scale uniformity, vias at the edge of the wafer now exhibit the same amount of erosion and dishing as those in the center.

8.6.1. SiO2 Surface Finish

One test was to polish a blanket coated SiO_2 wafer with the same conditions as those used in via damascene, Table 8-3. This was done to investigate the source of the CMP induced damage in the vicinity of the vias. An AFM of the polished surface can be seen in Figure 8.15. The surface is covered with many small scratches but not on the length scale of the damascened wafers, as a result the surface RMS has been reduced from 0.8nm to 0.2nm. It can be concluded that the scratches are caused by the abraded aluminium particulate. This would also explain why the scratches seem to originate from the vias. The abraded material is causing the star like scratch pattern.

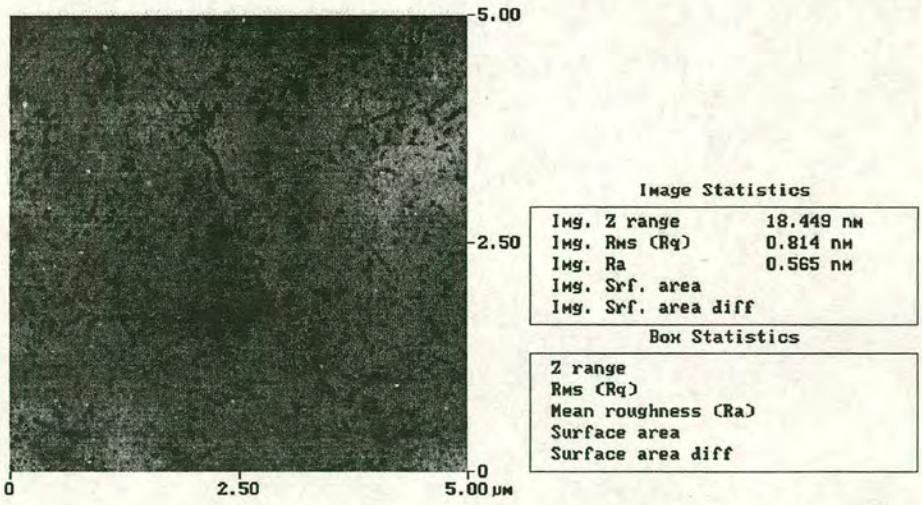


Figure 8.15 AFM image of the surface of a blanket SiO_2 wafer polished on a Rodel IC1000 pad and with Rodel QCT1010 slurry

8.6.2. Etch Rate Trials

The etch rate of the pre-metal deposition sputter clean could be used to determine the thickness of the CMP induced contaminated layer on top of the via. From the results of the etch trials, shown in Figure 8.16, it can be seen that the etch rate for aluminium is ≈1.2nm/minute and for SiO_2 is ≈0.84nm/minute. The etch rate is greater for aluminium than SiO_2 because sputtering is a physical process and so 'abrades' the softer aluminium faster.

The different magnitude of the error bars is due to the fact that the aluminium samples were measured with the Dektak, while the SiO_2 samples were measured using the Nanospec. Determining the small change in step height was difficult with the Dektak because it was working close to its limit of resolution. This made determining the etch step from the background 'noise' somewhat difficult, resulting in a large spread of readings.

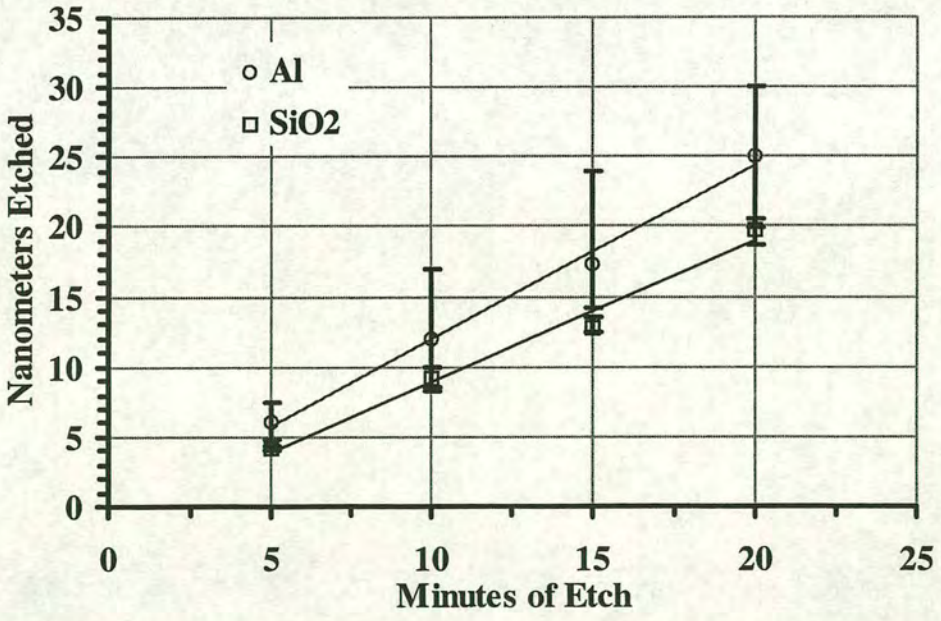


Figure 8.16 Graph showing sputter etch rates for SiO_2 and aluminium

8.6.3. Electrical Testing

The electrical testing was carried out on a HP4062B probe station. This was set-up by N. Rankin and D. Travis, without whose assistance the electrical tests could not have been performed.

The aim of the tests were to determine the minimum sputter clean time necessary to remove the CMP induced contamination layer. From this it will then be possible, knowing the etch rates, to make an informed assumption as to the thickness of this layer.

The tests were performed using a four point probe arrangement, two probes were used to drive the current through the via chain. Two more were used to measure the resulting voltage at each tap-off, and from this a resistance value calculated. All these measurements were carried out automatically resulting in a resistance value being displayed. As the measurements were extremely time-consuming it was decided that 5 sites for each etch time would be measured. These were then averaged and the error taken as the deviation from the average.

8.6.4. Electrical test Results

The results for zero etch time i.e. top level metal deposited directly onto vias which were subject to no pre-clean, have not been included. The resistance for these test structures measured mostly as open circuit or, where they could be measured, in GΩ's.

The results of etch times of 5, 7.5, 10, 15 and 20 minutes can be seen in Figure 8.17. The increase in resistance is due to the increased track length joining the individual vias. To remove the chain length dependency the average resistance per via at each chain length was calculated The result can be seen in Figure 8.18 and summarised in Table 8-4.

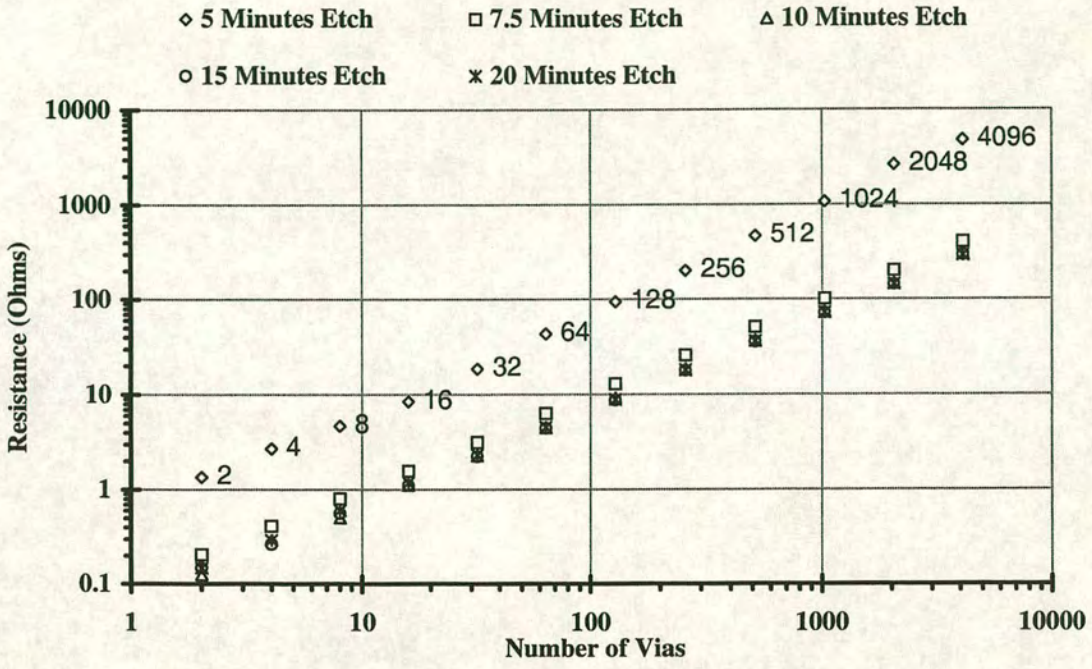


Figure 8.17 Resistance of vias for different sputter clean times

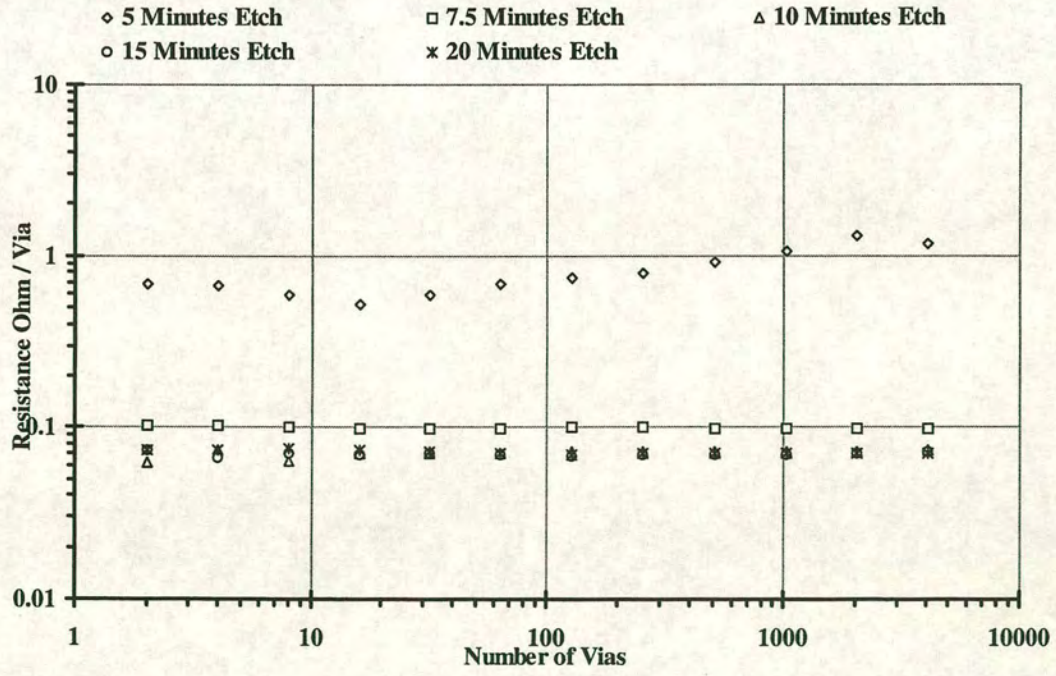


Figure 8.18 Average resistance per via at the different chain lengths measured

Etch Time Minutes	Average Resistance Ω	Error Ω	
		+	-
0			
5	0.8094	0.4894	0.2844
7.5	0.0998	0.0085	0.0067
10	0.0718	0.0033	0.0073
15	0.0698	0.0041	0.0033
20	0.0703	0.0027	0.0028

Table 8-4 **Average resistance per via for different etch times**

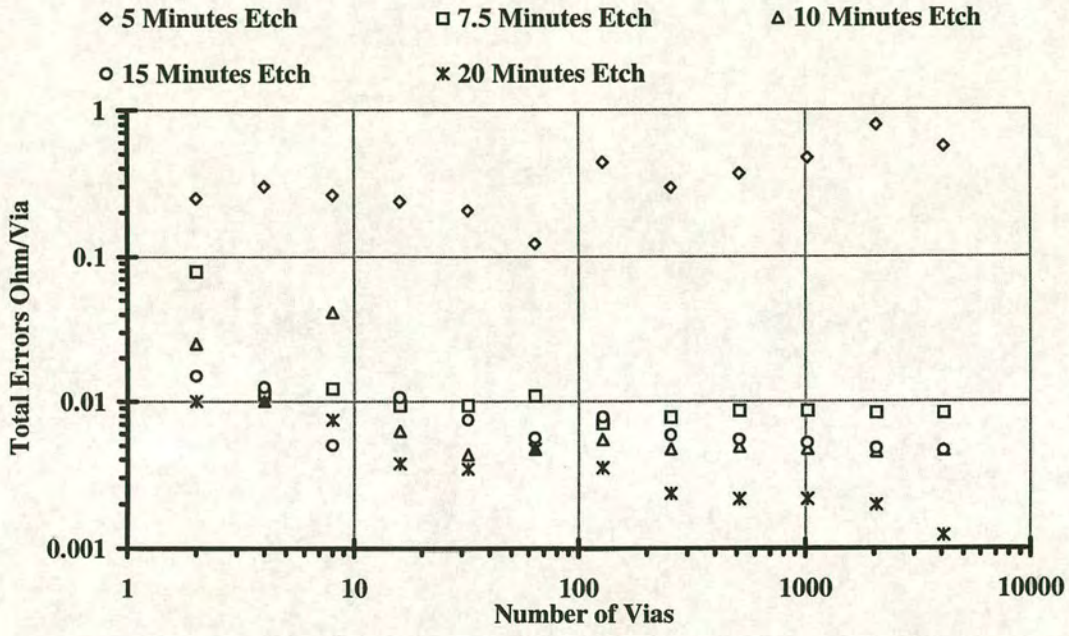


Figure 8.19 **Error per via at different etch times and chain lengths**

8.7. Conclusion and Comments

8.7.1. Dishing

Dishing of the vias was in the order of 50nm; this could be improved by the use of the post metal CMP SiO_2 buff to ≈14nm. This leads to benefits of decreased LC flow perturbation and of improved optical properties (Chapter 9).

8.7.2. SiO2 Surface Finish

The surface of the SiO_2 was also improved by the use of the SiO_2 buff step. It removed the damascene induced scratching and erosion producing a surface with an RMS of 0.2nm. It also removed the wafer scale polish uniformity problems, in that vias at the edge of the wafer had the same amount of erosion and dishing as those in the center.

8.7.3. Via Resistance

It can be seen that after 10 minutes of sputter-clean no further reduction in the via resistance is observed. This would indicate that, taking the aluminium sputter-etch rate to be 1.2nm per minute, a CMP induced contamination layer, thought to be Al_2O_3, of ≈12nm is present. This is about three times the native Al_2O_3 layer indicating that the mechanism of aluminium CMP is by the growth and removal of an oxide layer. A study by P. Wrschka *et al* [114], came to the same conclusion, but surprisingly calculated the Al_2O_3 layer to be between 2.2 and 3nm in thickness. This is lower than the generally accepted native Al_2O_3 thickness of between 3 to 4nm[109]. This leads to a contradiction as to how the induced Al_2O_3 layer can be thinner than the native Al_2O_3 layer. As soon as the wafer is removed from the polishing process, washed and dried, the native Al_2O_3 will be formed. Amazawa *et al*[115] found that there was a contamination layer, which covered the polished via, was in the order of 50nm in thickness. This layer not only included the induced Al_2O_3 but also slurry residue, this layer was totally removed by a CL_2/Ar pre-clean. It is obvious that the amount of Al_2O_3 and slurry residue on the surface of the vias will be different for each process used. It is therefore important to characterise any change in the process parameters thoroughly.

The resistance of the vias at different sputter-clean times can be seen in Table 8-1. It can be seen that the resistance falls to a low of ≈ 0.07Ω/via. This compares well with values of 0.7Ω/via reported by Schuck[116] *et al.* They produced via

chains of 1000μm in length with 2μm diameter vias etched into BCB, which had been used to planarise the underlying circuitry.

Although the via resistance did not decrease with sputter-clean times greater than 10 minutes the spread reduced, Figure 8.19 and Figure 8.20 (7.5 minute etch results have been omitted as they swamp out the rest of the data). This suggests that to increase yield a sputter-clean time of 20 minutes should be used.

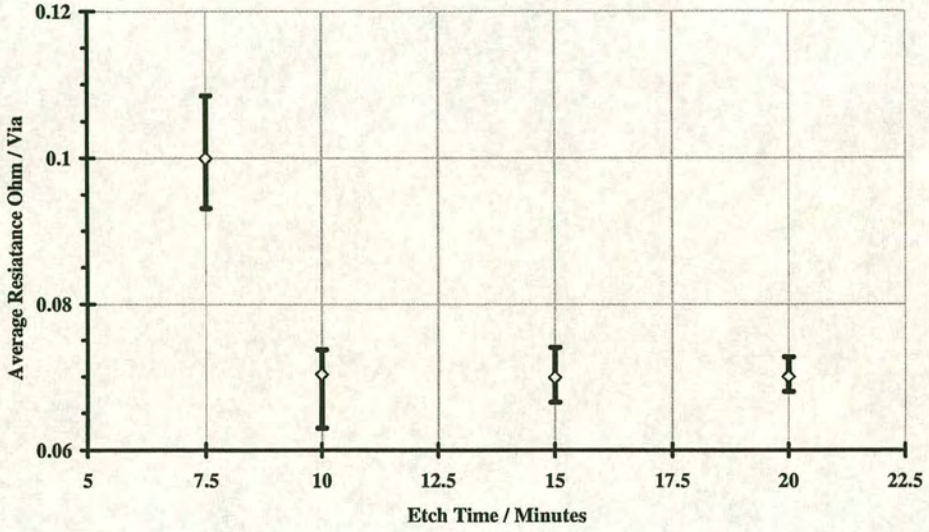


Figure 8.20 Graph showing error in Ω/via measurement

9. Liquid Crystal Flow Control

In the previous two chapters techniques to reduce, or remove, the mirror step height have been investigated. The use of the mirror damascene method produced mirrors buried within the dielectric surface but introduced problems of mirror dishing and array erosion. The use of the via damascene method, to produce co-planar vias, was also investigated. The via damascene method made it feasible to deposit 'thin' mirrors of typically 100nm in thickness. This was possible because the need to use thick, 1.5μm, metal to ensure electrical contact with the underlying circuitry has been removed.

The effectiveness of these different processing methods is now assessed with particular regard to their effects on LC flow front dynamics and final mirror quality. The two new methods are compared along with traditional 'thick' mirror and a thick mirror buff (enhanced conventional) technique.

A new technique of producing mirrors whose top surface are flush with the dielectric surface is also investigated[117]. This is termed the '**S**elf-aligning **I**nsulator **F**illed **T**rench'[118] (SIFT) process and is discussed in more detail later in this chapter.

The work in this chapter was carried out about equally between myself and Krishna Seunarine. Additional LC investigation was also done with the aid of Georg Bodammer.

9.1. Introduction

One of the more critical parts of the fabrication of high quality LCoS devices is a controlled means of introducing the liquid crystal into the gap formed between the silicon backplane and the coverglass.

If the LC flow is not uniform in its spatial extent, and the filling speed not tightly controlled, LC alignment defects are generated which affect the optical performance of the device in a detrimental way. In order to gain better control over the LC filling a process has been developed in which the inter-mirror trenches are filled with a dielectric material. This SIFT process is a variation on the lift-off process. It has been developed to fill the inter-pixel trenches, thus producing a smooth planar surface. We compare different surface preparation processes and demonstrate that it leads to even LC spreading, uniform LC alignment and a complete elimination of capillary pinning. The process also provides some insight into the nature of LC and surface interactions.

In addition to the problem of surface topography there is the added complication of different materials which the LC is forced to flow over during filling. The combination of the elevated mirrors and the different wettabilities of the two surface types (aluminium for the mirrors and silicon dioxide in the inter-mirror trenches) involved* leads to capillary pinning. This causes the LC to have a non-uniform flow-front during filling which in turn creates defects in the final LC alignment because the wetting conditions can determine the orientation of the molecule anchoring direction[119,120]. The problem is aggravated if SiO_2 alignment layers[121] are used[122]: Once the LC is introduced into the cell gap a realignment of the LC by heat annealing or other treatments (which are used successfully with polyimide alignment layers) to improve alignment uniformity is very difficult if not impossible. A method is needed of producing a planar surface with no recessed inter-mirror gaps and a fairly uniform wettability.

9.2. Experimental

To compare the LC flow fronts tests cells had first to be constructed. There now follows a brief description of the processing needed to make the test cells for each of the different processing techniques under investigation.

9.2.1. Backplane post-processing

Conventional Processing

The conventional process involves using CMP to planarise the dielectric surface above the underlying circuitry before the mirror elements are deposited. This planarisation step is common to all the processes described. It generates a very flat (10 nm over a 12 mm die) surface onto which the mirror elements are deposited[5].

In the conventional approach

1 Via contacts are etched through the ≈1μm thick planarised SiO_2 layer.

2 A blanket layer of ≈1.5μm of aluminium is sputtered onto the wafer to make good electrical contact to the drive circuitry below.

3 The aluminium is patterned with the mirror pattern and dry etched.

The process is illustrated in Figure 9.1*a*

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* The wettability is determined by the physico-chemical interactions of the respective surfaces and the liquid. It is conventionally quantified by contact angle measurements.

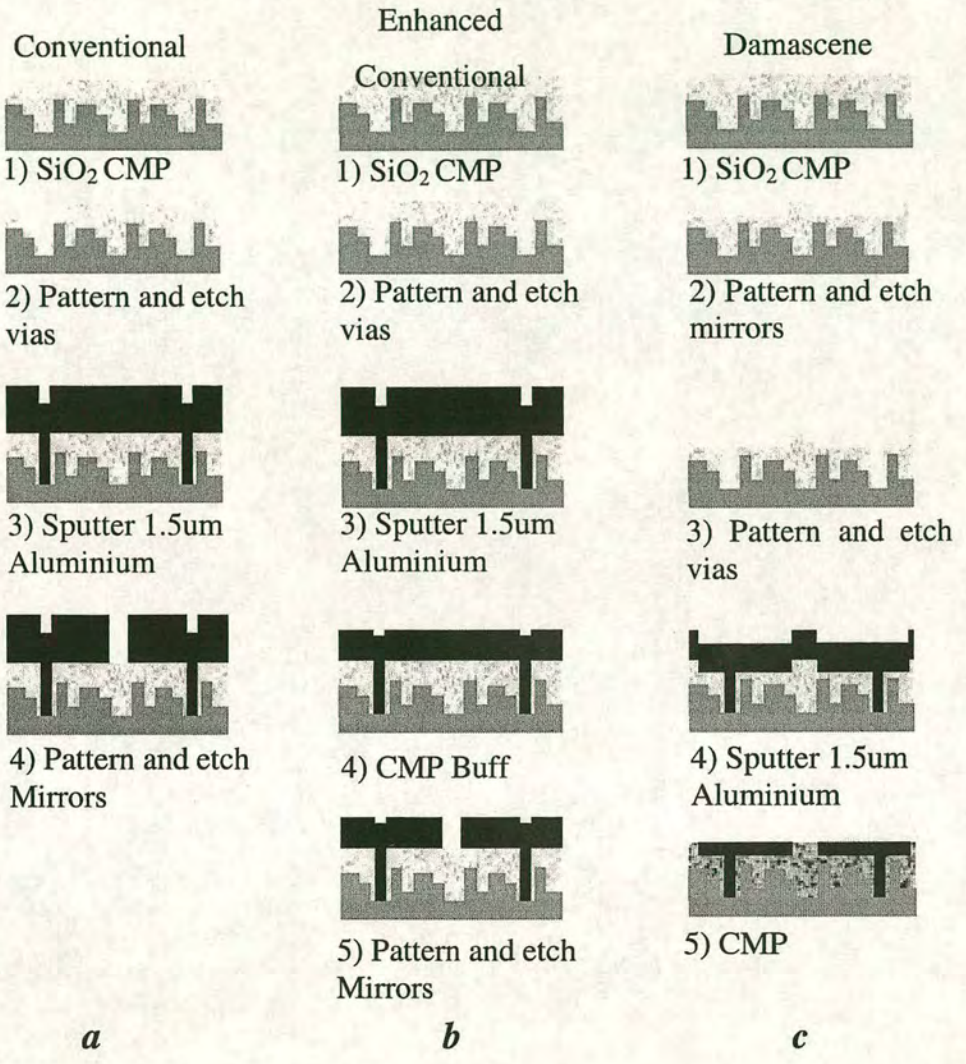


Figure 9.1 **Schematic of process flows for conventional (*a*), enhanced conventional (*b*) and mirror damascene (*c*) methods of LCoS SLM manufacture**

11. Enhanced Conventional Process

With the enhanced conventional process the sputtered 1.5μm of aluminium is buffed by CMP before mirror patterning. The buff uses a very soft pad in order to reduce the danger of scratching the mirror surface. It is used to reduce the surface roughness of the sputtered aluminium, and is not intended as a planarisation step, Figure 9.1*b*

Mirror Damascene Process

In this process first the mirrors, and then the vias are patterned into the planarised SiO_2 substrate. This creates mirror and via pits within the SiO_2 surface, aluminium is then sputter-deposited over the entire wafer surface completely filling them. CMP is used to remove the excess surface aluminium leaving metal only in the mirror and via pits. This process is outlined in Figure 9.1*c*.

Via Damascene Process

The via damascene process involves:

1. Patterning the vias into the planarised SiO_2 surface
2. Sputtering ≈1.5μm of aluminium onto the wafer, in an identical way to the conventional processing method.
3. CMP is now used to remove the surface aluminium, leaving it only in the via contact holes.
4. Depositing 100nm of aluminium
5. Patterning and etching of the mirrors

As there are now no step coverage concerns the process allows the deposition of a very thin (≈100nm) evaporated layer of aluminium. The thin aluminium is patterned, using dry etching. This process is outlined in Figure 9.2*a*.

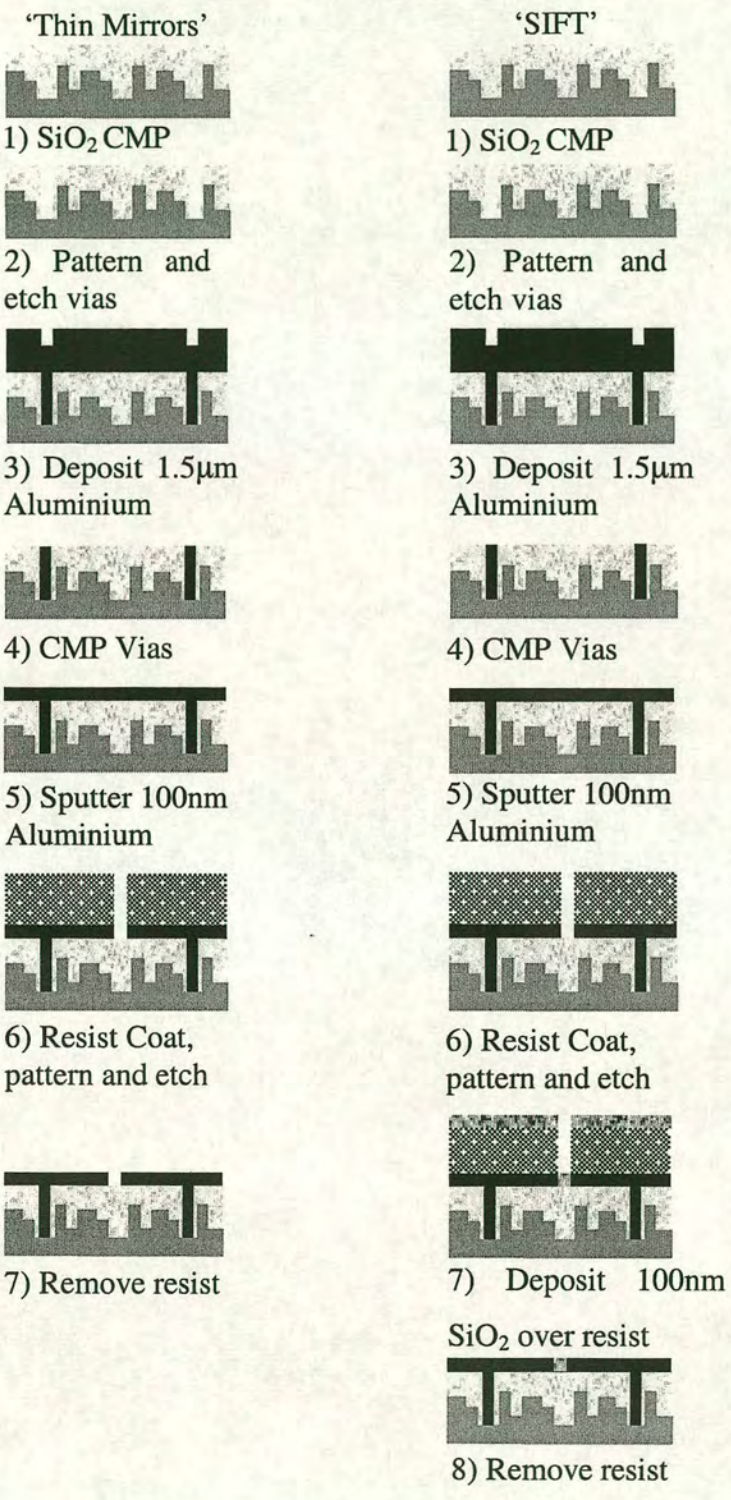


Figure 9.2 **Schematic of process flows for thin mirror (*a*) and 'SIFT' (*b*) methods of manufacture**

SIFT Process

The SIFT process[123], illustrated Figure 9.2*b*, is very similar to the thin mirror process, except that the resist used to pattern the mirrors is not removed. A 100nm layer of SiO_2 is now evaporated over the wafer. This covers the photoresist over the mirror elements but also fills the inter-mirror trenches. The resist, along with the unwanted SiO_2 overburden, above the mirror elements, is then removed in an ultrasonic bath while immersed in acetone. This leaves the SiO_2 between the mirrors filling the inter-mirror trench completely. The individual SIFT process steps are as follows:

1 Sputter deposit 100nm of aluminium using low power.
2 Spin-coat with 1.2μm photoresist (SPR2).
3 Photo-define mirror pattern.
4 Etch aluminium.
5 Deposit 100nm SiO_2.
6 Remove resist and SiO_2 overburden by ultrasonic agitation in acetone.
7 Rinse with de-ionised water.
8 Spin-coat with protective layer of photoresist and dice.

Two methods of silicon dioxide deposition were investigated, namely, evaporated and ECR PECVD. The evaporated SiO_2 was deposited at 0.75 nm s^{-1} at a residual pressure of 5 x 10^{-5} torr. A crystal monitor was used to determine the deposition rate. The ECR-PECVD oxide was deposited in an Oxford Plasma Technology reactor at a deposition rate of 0.45 nm s^{-1}.

9.3. Liquid Crystal Cell Construction

A 1.1mm thick cover glass, with ≈30nm of obliquely evaporated SiO_2 as the LC alignment layer[8], was used to construct test cells with the following substrates:

1 Conventionally fabricated backplane, with 1.5 μm-thick mirrors.

2 Enhanced processed (buffed mirrors)backplanes.

3 Mirror damascene backplanes.

4 Thin-mirror (Via damascene) backplanes.

5 Thin-mirrors with SIFT processed backplanes.

The LC cell gap was set by 3.1μm silica spacer rods mixed with UV curing adhesive (NOA88). The cells were filled with Merck E7 liquid crystal by capillary action and the flow fronts observed through an Olympus BH2 polarising microscope with crossed polarisers. All liquid crystal experiments were carried out at room temperature.

9.4. Results

9.4.1. Comparison Of Evaporated and ECR-PECVD

Atomic force microscope (AFM) images were taken of two samples, coated with evaporated SiO_2, and ECR-PECVD SiO_2, to investigate the surface topology of the filled trenches. The evaporated sample showed a very flat cross-sectional profile with 2.5nm rounding center to edge, Figure 9.3. There was also a small non-filled region between the mirror and the trench fill SiO_2 which appeared to be 12nm in depth and ≈50nm wide Figure 9.4. The actual extent of the gap is difficult to measure accurately due to the limitations of the AFM probe.

Although the trenches of the ECR-PECVD sample have been slightly over-filled it can be clearly seen in Figure 9.5 that it exhibits a greater degree of rounding (≈21nm). In addition to this rounding the unfilled area at the mirror oxide interface is much wider (100nm) and deeper (11.6nm) than the evaporated sample Figure 9.6. If the correct thickness (that is the thickness of the aluminium

mirror) of SiO_2 had been deposited then the side wall gap would have been much greater.

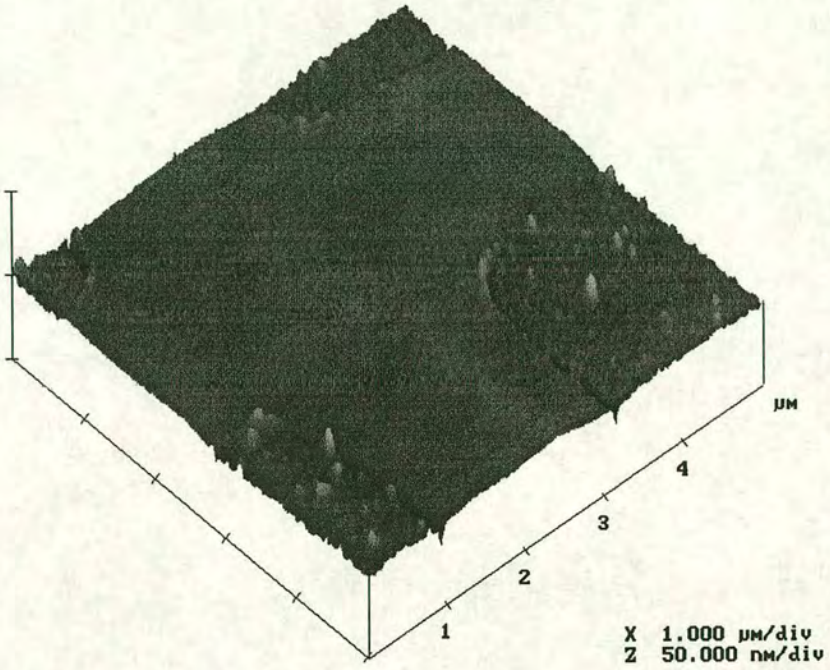


Figure 9.3 **AFM image of an intersection of four mirrors of a SIFT device filled with evaporated SiO_2**

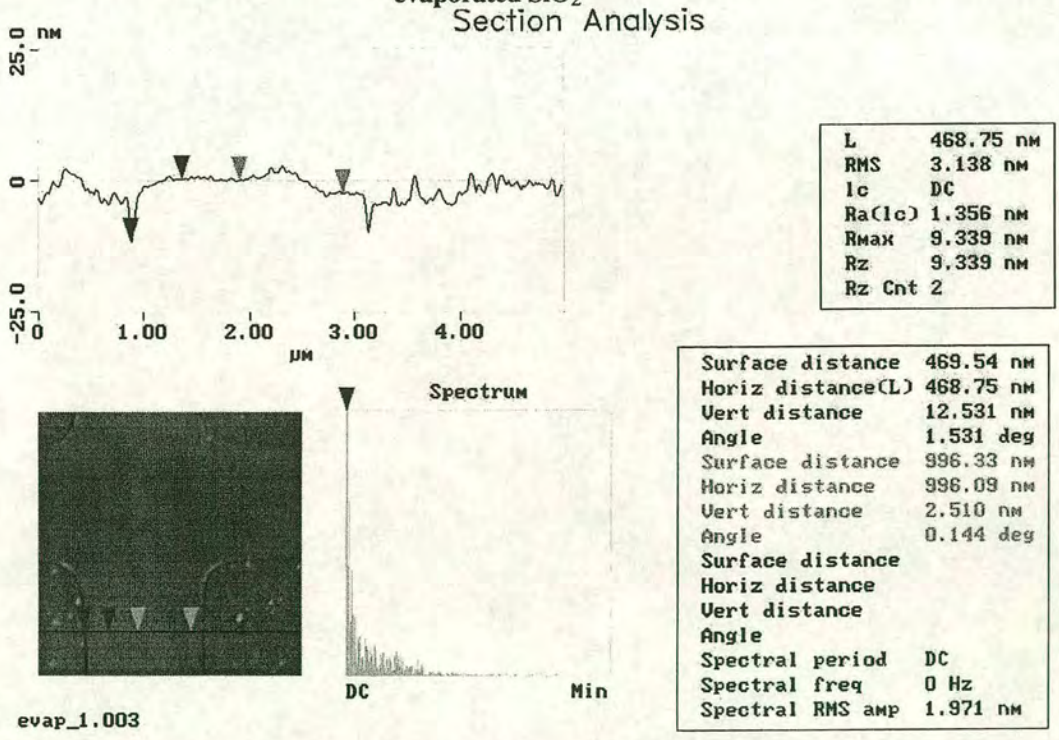


Figure 9.4 **AFM sectional analysis of an intersection of four mirrors of a SIFT device filled with evaporated SiO_2**

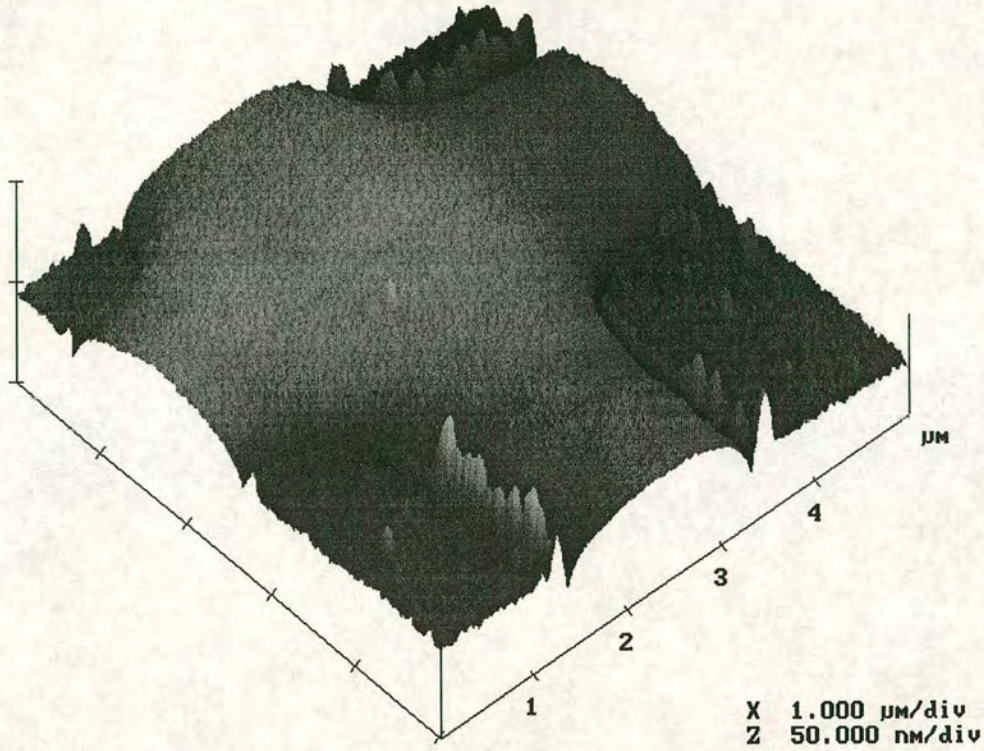


Figure 9.5 **AFM image of an intersection of four mirrors of a SIFT device filled with ECR PEVCD SiO_2**

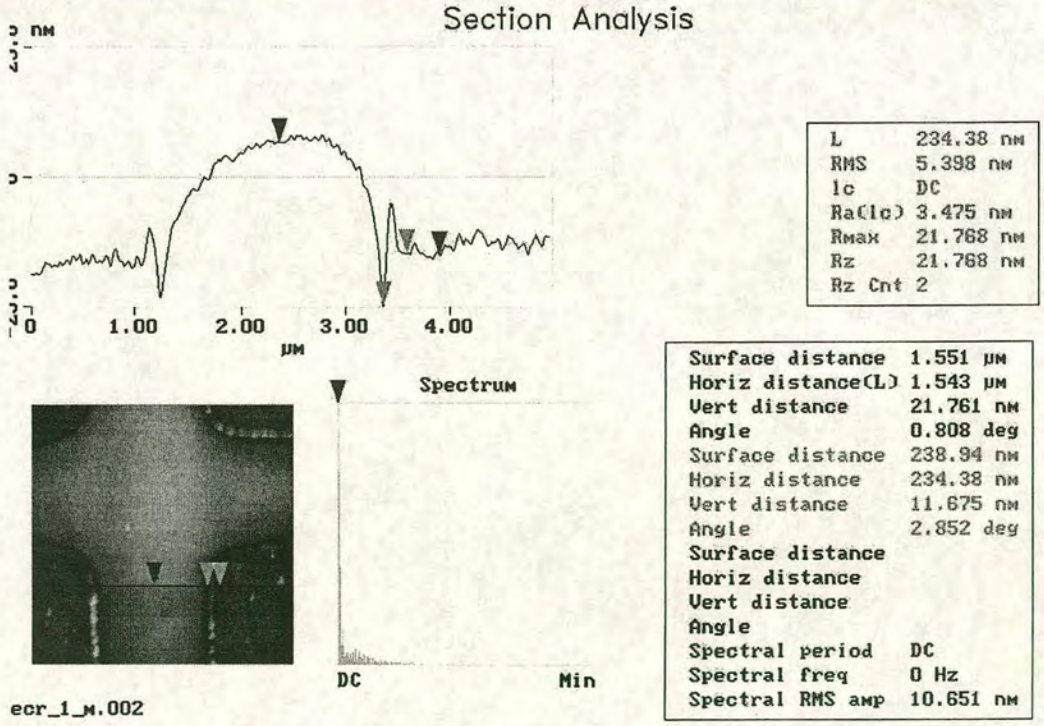


Figure 9.6 **AFM sectional analysis of an intersection of four mirrors of a SIFT device filled with ECR PEVCD SiO_2**

With the resist being deposited to a thickness of 1.2-μm, the evaporated SiO_2 did not completely cover the sidewalls. Although this discontinuous SiO_2 coverage allowed the removal of the resist in an oxygen plasma, it did not remove the excess SiO_2 deposited over the mirror region. The result of an oxygen ash for 60 minutes can be seen in Figure 9.7. Incomplete SiO_2 removal is clearly evident.

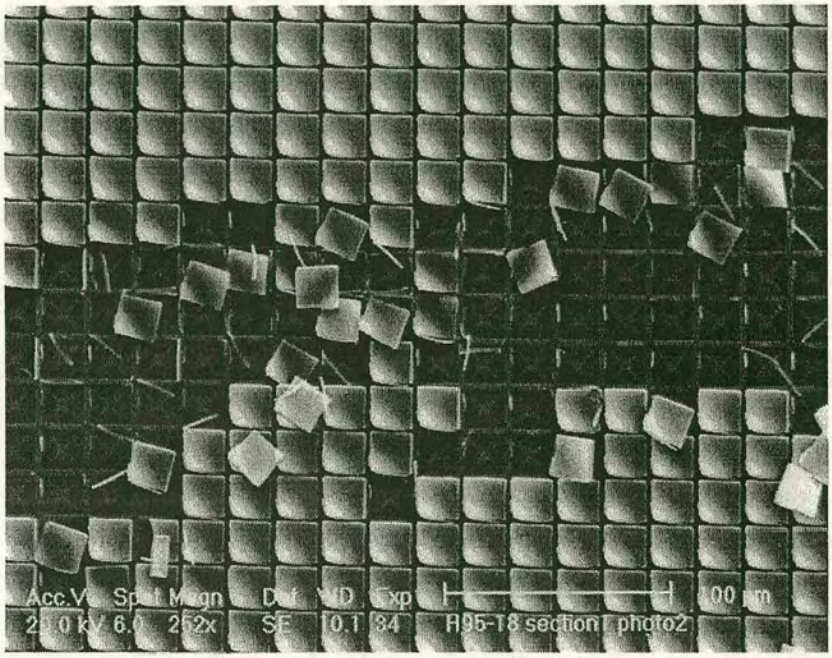


Figure 9.7 **SEM image of SIFT device after removal of photoresist in oxygen plasma for 60 minutes**

The 'X' seen within each mirror is thought to be the result of resist residue trapped under the SiO_2 'roof'. Ultrasonic agitation in acetone, which was not observed to damage the underlying silicon circuitry, was found to be necessary to break-up and disperse the SiO_2 overburden completely, as shown in Figure 9.8.

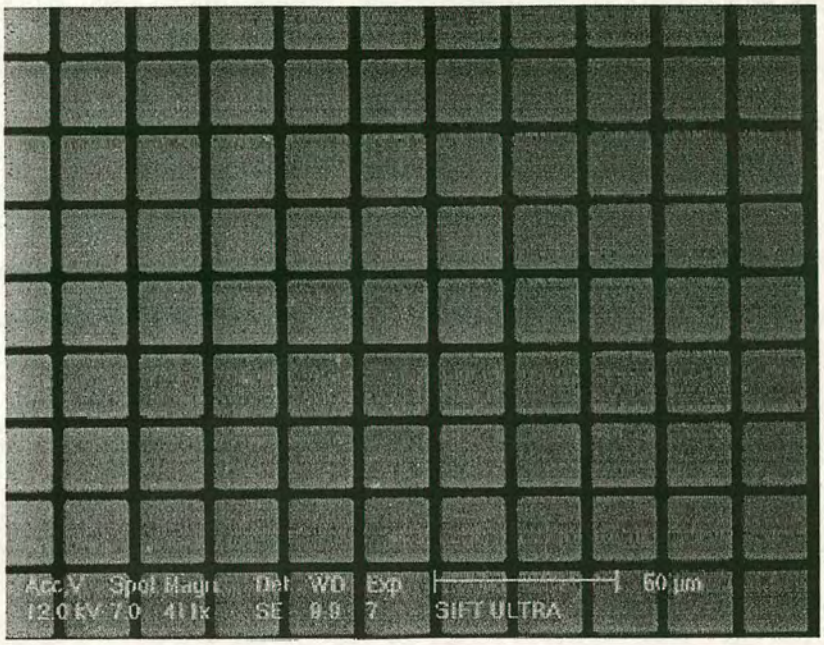


Figure 9.8 **SEM image of SIFT device after removal of photoresist with ultrasonic in acetone for 10 minutes**

It is interesting to note that there is a small amount of uncleared SiO_2 on the ECR-PECVD sample even after cleaning, Figure 9.5. This is material deposited on the bottom of the sidewall of the resist. ECR-PECVD deposits a much more conformal layer than evaporation. This explains the greater amount of SiO_2 residue left at the side of the filled trenches in the ECR-PECVD samples.

The SiO_2 deposition rate using, ECR PECVD, was observed to be 30% higher in the field region than in the inter-mirror gaps, this led to a step at the array-field boundary. This is thought to be due to a shrouding effect, produced by the trench depth, causing a depletion of gas reactants in these areas leading to a lower deposition rate. It is also probable that this shrouding effect is the cause of the pronounced rounded profile of the deposited material.

The sample with evaporated SiO_2, Figure 9.3, showed no differential deposition rate between array and field. Being a physical deposition technique there are no reactant gasses to become depleted within the trench so the deposition rate remains constant. Gross shadowing of the depositing flux by the resist walls

was not evident in the samples (apart from the small uniform gap between SiO_2 trench filled material and the mirror sidewall).

The deposition uniformity of both evaporated and ECR PECVD SiO2 was measured on 100mm diameter wafers. The normalised results of the SiO_2 uniformity can be seen in Figure 9.9.

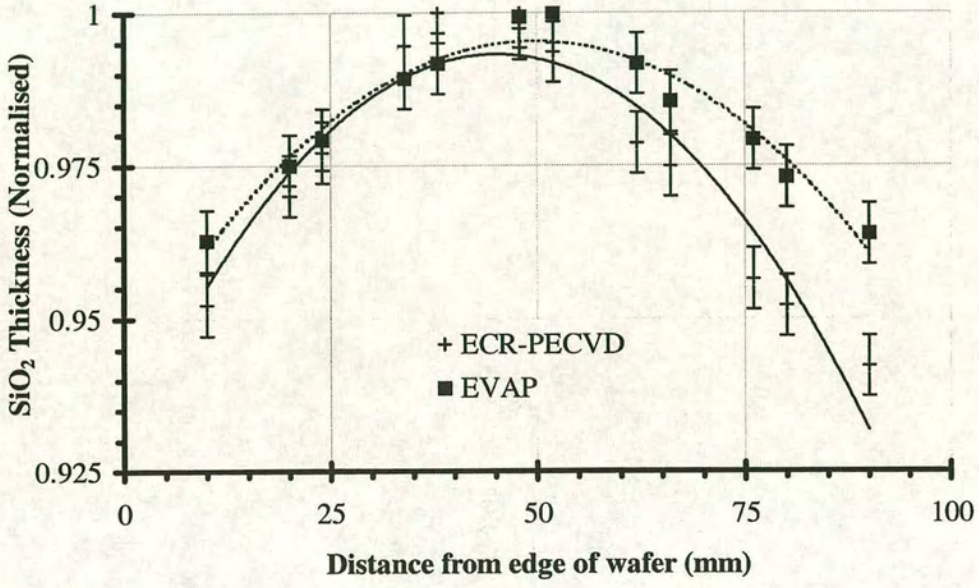


Figure 9.9 **Normalised deposition uniformity of evaporated and ECR PEVCD SiO_2 on a 100mm wafer**

ECR-PECVD deposited SiO_2 exhibited a centre fast deposition, with a uniformity of 3.2%. Evaporated oxide had a uniformity of 2.1%, which was also centre thick.

9.5. Liquid Crystal Cell Filling

Important factors which influence the final alignment of the LC after cell filling include:

1 LC cell filling speed,
2 LC flow front direction,
3 Substrate topology
4 Substrate material

During the injection of LC into the cell, the local capillary forces (which are influenced by the local cell gap spacing and physico-chemical properties of the enclosing surfaces) cause the LC flow front to deviate from its ideal linear shape. This non-ideal LC flow front shape causes an inhomogeneous alignment texture that reduces the contrast ratio in the finished device. A more detailed description of this phenomenon and its effects on device performance can be found in Cox[124] and Bodammer[125]. A summary of the results is shown in Figure 9.10 detailing surface finish and LC fill flow front.

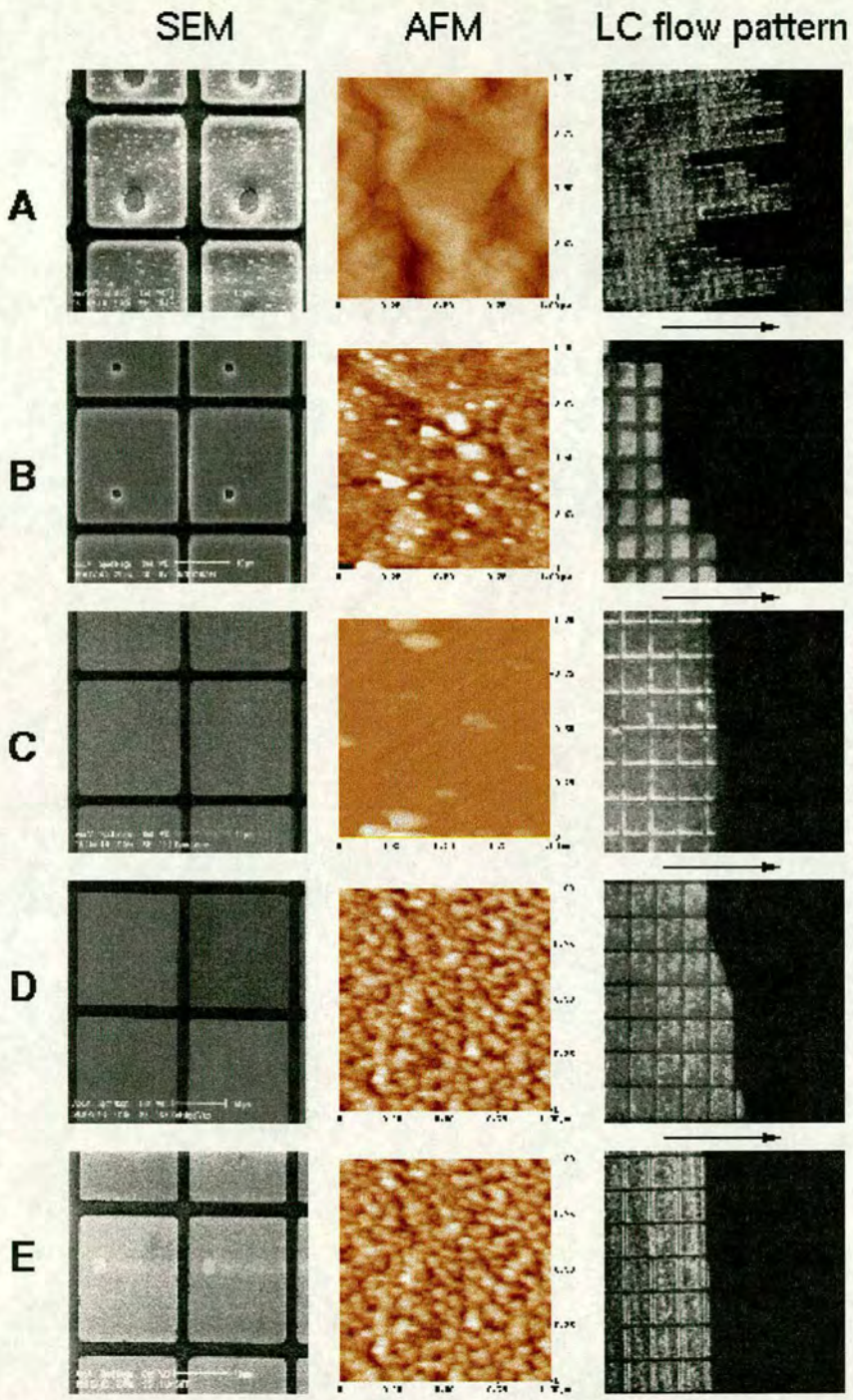


Figure 9.10 Effect of processes on surface finish and LC flow characteristics (LC filling from left to right as indicated by the arrow). See also table 1. Column one shows SEM images of the backplanes, column two 1μm square AFM images of one aluminium pixel, and column three shows the respective LC flow character. A indicates the result of the conventional process, B of the enhanced conventional process, C of the damascene process, D of the thin-mirror process, and E of the SIFT process. The peak heights in the AFM images are A -- 103 nm, B -- 10 nm, C -- 76 nm, D -- 8 nm, and E -- 8 nm.

9.6. Results and Discussion

9.6.1. Conventional Processing

Cells constructed with the conventional backplanes were observed to fill with a flow front that drastically deviated from the ideal linear front due to the effects previously described, Figure 9.10*a*. The LC tended to flow from one pixel to the next in the x-direction, rather than to adjacent pixels in the y-direction. The LC director tends to align parallel to the flow front. This causes the surface tension parallel to the flow front to be smaller than the surface tension perpendicular to it. Thus, flow parallel to the mean flow front is preferred to flow perpendicular to it.

9.6.2. Enhanced Conventional Processing

The surface finish of the thick mirrors was greatly improved by CMP buffing. Upon observing the LC flow front during cell filling it was seen that the flow front no longer propagated in the peculiar manner observed in the previous example. However, there was still a significant disruption to the LC flow front during cell filling Figure 9.10*b*.

The process reduces the via dimple size and thus increases the mirror fill factor. Reducing surface roughness also improves surface reflectivity according to Equation 9-1.

$$\frac{R}{R_o} \cong \left(\frac{4\pi\delta}{\lambda}\right)^2$$

Equation 9-1 Equation showing relationship between surface roughness and reflectivity where R is the specular reflectance of the surface, R_0 is the fraction of the incident light which is scattered, δ is the rms height of the surface irregularities, and λ the wavelength of the incident light[126]..

A summary of the aluminium surface roughness, after the respective processing, can be found in Table 9-1.

Deposition Method	Film Thickness nm	RMS Roughness nm	
		10 μm^2 scan	1 μm^2 scan
Evaporated	100	1.071	1.144
Sputtered	100	4.758	5.291
Sputtered	1500	35.415	15.438
Sputtered and polished (hard pad)	1500	17.792	5.649
Sputtered and buffed (soft pad)	1500	8.864	0.840

Table 9-1 AFM calculated surface roughness of mirrors produced by different processing methods.

9.6.3. Mirror Damascene Processing

Although unsolved problems such as mirror dishing/scratching and array erosion hinder the adoption of the damascene process, the LC flow front over the array was seen to be greatly improved, compared with the conventional and buffed conventional mirrors, as is shown in Figure 9.1B. While the damascene process reduced the LC flow front disturbance, dishing and array thinning were observed to cause a variation in LC layer thickness. The latter effect manifests itself by colour variations across the device.

9.6.4. Via Damascene Processing

The LC flow front on the thin mirror backplane still suffered slightly from the capillary effects described earlier, but to a much lesser extent than before Figure 9.10*d*. Aluminium films become effectively optically opaque at a thickness of ≈60 nm[127]. This determines the lower limit of mirror element thickness. Although the thin mirror process reduced the inter-mirror trench depth from 1.5 μm to much less than 0.1 μm, it did not remove capillary pinning completely.

9.6.5. SIFT Processing

The cells constructed from backplanes with SIFT processed thin-mirrors were then filled. The LC flow fronts were observed on both a pixel and macroscopic scale in cells which were filled:

1 parallel with respect to the pixel mirror edges

2 diagonally with respect to the pixel mirror edges

The LC flow fronts, in both cases were seen to propagate over the patterned substrates with no disruption to their shape as shown in Figure 9.11

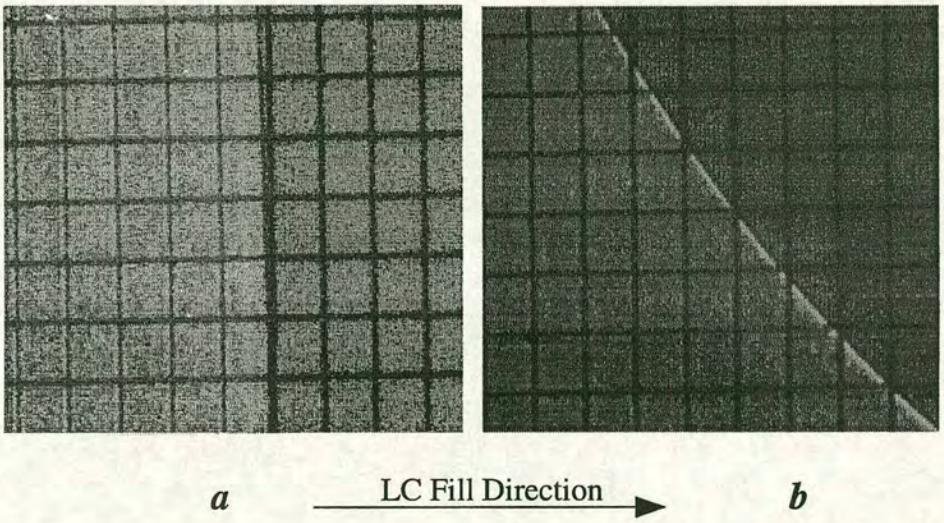


Figure 9.11 LC filling of a SIFT processed device showing filling at right angles to mirrors, *a*, and at 45° *b*

9.6.6. Physico-Chemical Effects

The effect of the substrate material on the LC flow front was also investigated. A wafer coated with 30nm of evaporated aluminium was patterned to form a grating structure. LC test cells were then constructed:

1 With the LC alignment layer on the coverglass only

2 With the LC alignment layer on the coverglass and silicon backplane.

The cells were then filled with LC, as before, and the flow fronts observed. The speed of propagation of the LC flow front depended on the substrate material: The LC wetted the aluminium strips preferentially, as shown in Figure 9.12A with alignment on the coverglass only and Figure 9.12B with alignment layer on coverglass and backplane.

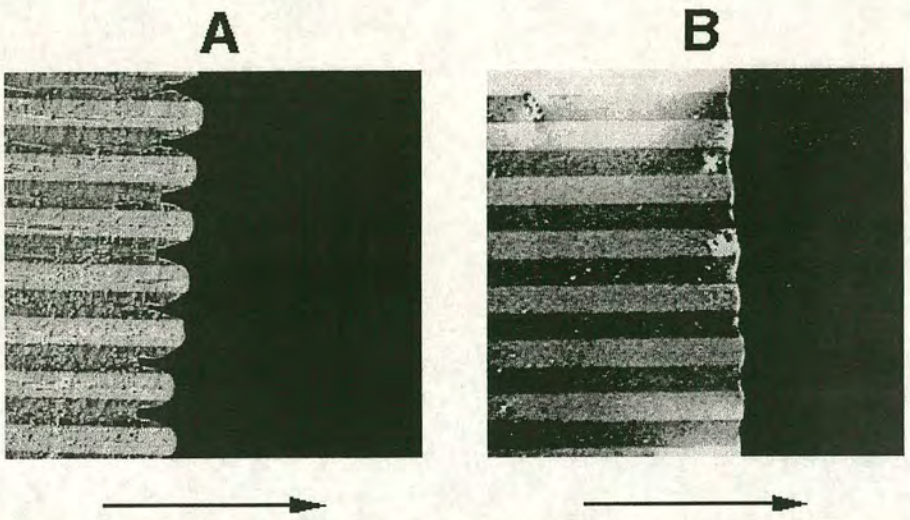


Figure 9.12 Illustration of the physico-chemical effect: NLC (E7) flow front (flow is proceeding left to right) over a 30nm thick 100μm wide aluminum grating (A) without a SiO_2 alignment layer over the backplane and (B) with a SiO_2 alignment layer over the backplane. LC propagation speed on bare aluminium: 114.2μm/s, propagation speed on bare silicon dioxide: 93.7μm/s.

The LC progressed across the aluminium at a speed of 114.2 μm s^{-1}, whereas it flowed over the silicon dioxide at only 93.7 μm s^{-1}. The difference in wettability of the silicon and the aluminium can have two origins. Firstly, as shown in Figure 9.3, the aluminium is rougher than the evaporated SiO_2 in the trenches. In other words roughness enhances wetting, which has also been predicted by Chow[128]. Secondly, it could indicate that the aluminium surface has a higher surface energy than the evaporated SiO_2. This in turn would also mean that the LC wets the aluminium preferentially.

Coating the coverglass with a LC alignment layer reduced the difference in wettability of the aluminium and silicon dioxide strips only slightly. Application of the alignment layer to the backplane, however, reduced the difference between the wettabilities almost completely. Unfortunately, this does not clarify what the origin of the effect is (i. e. a difference in surface energies of the aluminium and silicon dioxide or caused by the different surface roughness).

9.7. Conclusions and Comments

In this chapter different surface preparations in terms of their effect on liquid crystal flow front aberrations have been compared. New process of forming mirrors, by combining and customising some of the conventional post-processing techniques have been developed. The SIFT processing procedure, which requires no additional masks, shows great promise in test cells constructed and filled with NLC. The liquid crystal flow front, which is so important in determining the alignment of the LC in the cell, has been shown to maintain its desired linear shape when the new process is used. We have shown that the mirror quality depends both on the metal deposition procedure and the subsequent processing. Post-CMP particulate contamination was observed despite a rigorous cleaning. This causes a degradation of the surface quality, leading to lower reflectance and potentially poorer LC flow and alignment.

Although evaporated aluminium had a lower surface roughness than sputtered aluminium, Table 9-1, sputtered aluminium will still be used for device fabrication. This is because of the inability of the Edinburgh University's evaporator to perform a pre-metal deposition sputter clean. A sputter clean essential in the production of low resistance damascened vias, Chapter 8.

10. Conclusions, Discussions And Future Work

In the following Chapter my work, and the main results, will be discussed and conclusions made. In the main my research has involved the use of CMP, for both dielectric and metal, the primary goal being to minimise the surface topography of LCoS SLM devices. The two main reasons for this were the need to improve both the optical quality of the device and the final LC alignment quality.

My time has been divided almost equally between the investigation of dielectric and metal CMP. Each technique improves the device in a number of different ways, which will be discussed.

Some of the work I have been involved with overlaps with the remit of other projects'. As these project will continue past the end of my PhD so too will the work started, as such some of this work remains unfinished. Towards the end of my PhD I have been investigating, with George Bodammer, the non-flatness of the device backplanes, and attempting to separate the contributions from circuitry induced and wafer induced die warp. A new device manufacture process flow is also being investigated, the main advantages of which will be highlighted.

10.1. Dielectric Planarisation

My research on SiO_2 CMP has built upon the early work done within the Applied Optics and Microfabrication groups. Although the viability of CMP was demonstrated to improve LCoS device quality, several issues were never totally resolved, the main being that of array 'doming'. The 512^2 device is comprised of a central raised area of densely packed features, the array, surrounded by a lower feature density area, the field. This layout adversely affects the device polishing characteristics (Chapter 4). The dynamics of CMP results in the array being 'seen'

as a single very large feature, as such the edges are polished more quickly than the centre, resulting in a 'domed' profile. My work showed that once this profile has been established further polishing merely reduces the dielectric thickness and does not further alter its shape. In tests it was found that the SiO_2 at the centre of this dome could be as much as 0.3μm thicker than SiO_2 at the edge (Figure 4.8). To remove the doming problem a pre-CMP SiO_2 etch, to modify the initial array step height, was devised. It consists of photo-defining a 'window' in the photoresist over the array region (Figure 4.11), the exposed array is then etched to reduce the thickness, and hence the step height, of the SiO_2. This technique makes it possible to modify the initial step height in such a way, that after CMP, the array had been completely removed. The optimum pre-CMP array step height was found to be 0.8μm above the field region. Using this technique it was possible to produce an SiO_2 thickness uniformity, across the 10mm array, of 10nm (Figure 4.13).

The post-CMP uniform SiO_2 thickness over the array results in all surface topography being removed, both the individual features and the array step/profile. As all surface topography has now been removed it allows for either the deposition of 1.5μm thick mirrors or to allow further processing using metal CMP.

10.2. Metal CMP

The next objective was to remove the mirror step height associated with 'conventional' dielectric CMP processing. Although the dielectric has now been planariesed adding the mirror layer creates new surface features. The presence of these features adversely affects the LC filling characteristics which, in turn, degrades the final LC alignment quality. The mirrors, on conventionally processed backplanes stand proud of the surface by as much as 1.5μm. This mirror step height is large enough to perturb the LC during cell filling, it is therefore desirable that it is minimised. To achieve this dual (mirror) damascene and single (via) damascene methods were investigated.

Initial tests were performed using a specially designed mask, which consisted of a variety of feature sizes and densities (Figure 6.1). The outcome of these tests was to establish that the softer Polytex pad was unsuitable for aluminium CMP. Although it produced a scratch free surface the amount of dishing and erosion induced were unacceptable. To overcome these drawbacks a harder IC1000 stacked pad was used, which is the same pad as used for SiO_2 CMP.

During the trials, using the tests pattern and IC1000 pad, useful information was learned as to the source of CMP induced damage. The severe scratching encountered was traced to several sources, the main culprits being slurry particle agglomerates and pad asperities. It was found that if high head pressures were used wafer/pad contact resulted in a severely scratched surface. To alleviate this the head pressure was lowered and a new pad conditioning regime developed. These two modifications resulted in a vastly improved surface finish with little sign of scratching and producing a highly specular surface. Metal slurries are prone to 'ageing', in that the sub-micron particulates tend to agglomerate and form far larger particulates, which can be up to tens of microns in size (Figure 7.3). In an attempt to remove these, the slurry was allowed to settle, after mixing with the hydrogen peroxide oxidising agent. It was then decanted into another container leaving the larger particulates behind in the 'sludge' at the bottom. Although this helped it is thought the only reliable method to remove the large particles would be by the use of in-line filtration.

The polishing of the test pattern was then carried out to investigate the parameters which affect feature dishing and dielectric erosion. The conclusion was that dishing is strongly linked to feature size but only weakly linked to the feature density. The parameters affecting the amount of CMP induced dielectric erosion appear to be more complicated. Many authors state that the pattern density is the only cause of erosion, this is a somewhat over simplification. For the same pattern density different amounts of erosion were observed (Figure 6.21). This leads to the conclusion that erosion is a product of more than one factor. The critical factor appears to be not pattern density (the ratio of 'up' topography to 'down' topography) but to feature density (how many 'up' areas in a given unit

length). The size of these 'up' areas also appears to influence the amount of dielectric erosion, as does the total extent of the patterned area.

10.2.1. Mirror Damascene

After these initial tests had been completed the development of a dual damascene aluminium process was investigated, Chapter 7. This method produces mirrors whose surface is level with the surrounding dielectric surface, this results in a reduction of LC flow front irregularities. Unfortunately this technique introduces a new set of problems, The main being array dishing due to SiO_2 erosion, although others exist namely individual mirror dishing and degradation of the mirror surface due to scratching and particulate contamination. These were minimised using a pre-CMP etch to remove the aluminium in the field area, (Figure 7.6) negating the need for a long over-polish period to clear this area. Although this technique reduced the array erosion, and dishing, by 50%, via damascene produced devices with far less CMP induced degradation.

10.2.2. Via Damascene And Thin Mirrors

Via damascene has been found to have a number of advantages over the mirror damascene method, Chapter 8. Via damascene produces vias which are level with the dielectric surface, this vastly reduces any metal step coverage concern so allows thin, 100nm mirrors, to be deposited.

With conventional processing the via and mirror metal are the same layer. The mirror metal therefore has to be of sufficient thickness to fill the ≈1μm deep via and make contact to the underlying circuitry. It is therefore necessary that the final mirror metal is ≈1.5μm thick. In addition to this to ensure adequate metal step coverage the metal has to be deposited at high power (Figure 8.7) which results in a rough mirror surface. The poor mirror finish further degrades the LC flow front, by seeding defects, and also increases unwanted light scattering from the mirror surface.

A major concern when developing the via damascene technique was the possibility of high contact resistance between the polished via surface and the final mirror metal layer. To investigate this via chains were designed and manufactured. Theses were then subjected to various pre-mirror metal deposition clean times. The cleaning method was by the use of argon atom bombardment, which can be carried out within the same vacuum chamber as the metal deposition. This allows cleaning and metal deposition to be done concurrently without the vacuum being broken, and thus the surface re-oxidising. These tests confirmed the presence of a CMP induced contamination layer. Using the known sputter etch rate of aluminium (Figure 8.16) and the resistance measurements, (Figure 8.18) it was possible to estimate the thickness of this layer. The CMP induced contaminated layer is in the order of 12nm in thickness so by removing this amount of material it was possible to substantial reduce the post-CMP via contact resistance from GΩ/via to ≈0.07Ω/via (Table 8.4).

As with the mirror damascene method problems of erosion and dishing were encountered, although to lesser extent. The problem of CMP induced dielectric damage manifested itself as erosion localised around the vias and a 'globally' degraded surface finish. As the final mirror thickness was ≈100nm it 'mimics' the underlying surface topography. The CMP induced damage therefore degraded the final mirror quality. To overcome these problems a post-damascene buff was used, it consisted of using SiO_2 slurry and low speeds/pressures to remove a few tens of nanometers of the damaged surface. A two minute buff was sufficient to remove all dielectric surface damage and reduce via dishing from ≈50nm to <13nm. The global dielectric surface finish was also improved with a final surface finish of ≈0.5nm RMS roughness.

Via damascene also has another less obvious advantage, that of reduced particulate contamination. Metal CMP slurry residues are particularly difficult to remove from aluminium surfaces while they are relatively easy to remove from SiO_2 surfaces. The mirror damascene structures have a very large aluminium surface area, which can lead to a particulate contamination problem. These particulates tend to degrade both the optical quality and LC fill dynamics. Via

damascene, on the other hand, has a far smaller final aluminium surface area, which reduces the problem. The post-CMP SiO_2 buff further helps to remove any slurry residue, resulting in a cleaner surface.

With the reduction of the step coverage concerns it is now possible to deposit a thin final metal layer. The surface roughness of the metal is a function of thickness and deposition power. By depositing a thin layer at low power the best surface finish can be achieved.

The use of the via damascene technique is recommended in preference to the mirror damascene technique because of the following benefits:

1. No array erosion problems
2. No mirror dishing
3. Better final mirror quality (thin mirrors)
4. No additional masks needed
5. Less concerns with post-metal CMP contamination

10.3. LC Flow Investigation

One of the main reasons for producing a smooth featureless surface is to improve the alignment quality of the LC. During cell filling the LC is drawn between cover the glass and backplane by capillary action. As the LC flows over the back plane the flow-front is disrupted by any surface topography encountered. The final alignment quality of the LC is a direct function of the initial flow front characteristics. To improve the final LC alignment it is imperative to reduce the surface topography as much as possible.

In order to confirm that by reducing the surface topography the LC fill flow front was improved test cells were constructed, Chapter 9. To compare different back plane morphologies several manufacturing techniques were investigated.

The techniques were:

1 Conventional processing
2 Enhanced processing
3 Mirror damascene
4 Via damascene
5 Self-aligned Insulator Filled Trench (SIFT) processing

The manufacturing process for each backplane type is shown in Figure 9.1 and Figure 9.2.

All the processing methods showed a more uniform LC flow front than the conventional technique, with the SIFT method showing the least disruption.

The SIFT method uses a lift-off technique to fill the inter-mirror trenches with evaporated SiO_x to produce a planar surface (Figure 9.3). The use of this method is only feasible because via damascene makes it possible to deposit a thin final metal layer. Without thin mirrors a lift off technique would not be possible because the thickness of SiO_x necessary to fill the inter-mirror trenches would make it impossible to remove the overlying photoresist.

The results proved that by reducing the surface topography the LC flow front can be controlled and made to flow in a more uniform manner. This will aid in improving the final LC alignment quality.

10.4. Ongoing And Future Work

There are a number of investigations currently underway at the time of writing this thesis. As they are being done in combination with other projects, which continue past the end of my PhD, they will not be finished before this thesis's completion. All investigations are in collaboration with George Bodammer and will be completed by him.

These projects are showing great promise and should result in improved devices. The first is concerned with backplane flatness the second with processing. They are detailed in the subsequent sections.

10.4.1. Backplane Flatness

SLM back-planes have been known to suffer from some degree of die warp. What was not known was the true extent, or the source, of this phenomenon. Its origins could be from stresses induced in the fabrication of the devices. The wafer goes through many heating and cooling cycles and has many different types of films deposited on them, each with its own associated stress component. Wafers themselves are not truly flat but have some intrinsic warp of their own. Myself and George Bodammer devised a method to assess the contribution of the circuitry induced warp and the wafer induced warp.

To separate circuitry and wafer induced bow the following methodology was used:

1 Using a white light interferometer individual dies were imaged
2 Remove circuitry by wet etching
3 Re-image same die

By imaging the same die in the same orientation with and without the circuitry the two sources of device warp can be separated. To avoid the problem of the circuitry topography influencing the imaging all imaging was carried out on the back of the die.

The above methodology was used to investigate the 64^2, 176^2, 256^2, 512^2 and the 1024^2 devices, with 3 samples of each being used. The results showed that after removal of the circuitry the amount of die warp was, in all cases, reduced. The results for a typical 512^2 device can be seen in Figure 10.1.

It is evident that the circuitry induces some of the observed warp. Each device type exhibited approximately the same degree of warp. The fact that the every die, of the same device, has the same level of warp means that wafer scale flattening may be possible. The method presently under investigation involves depositing a stressed film on the backside of the wafer.

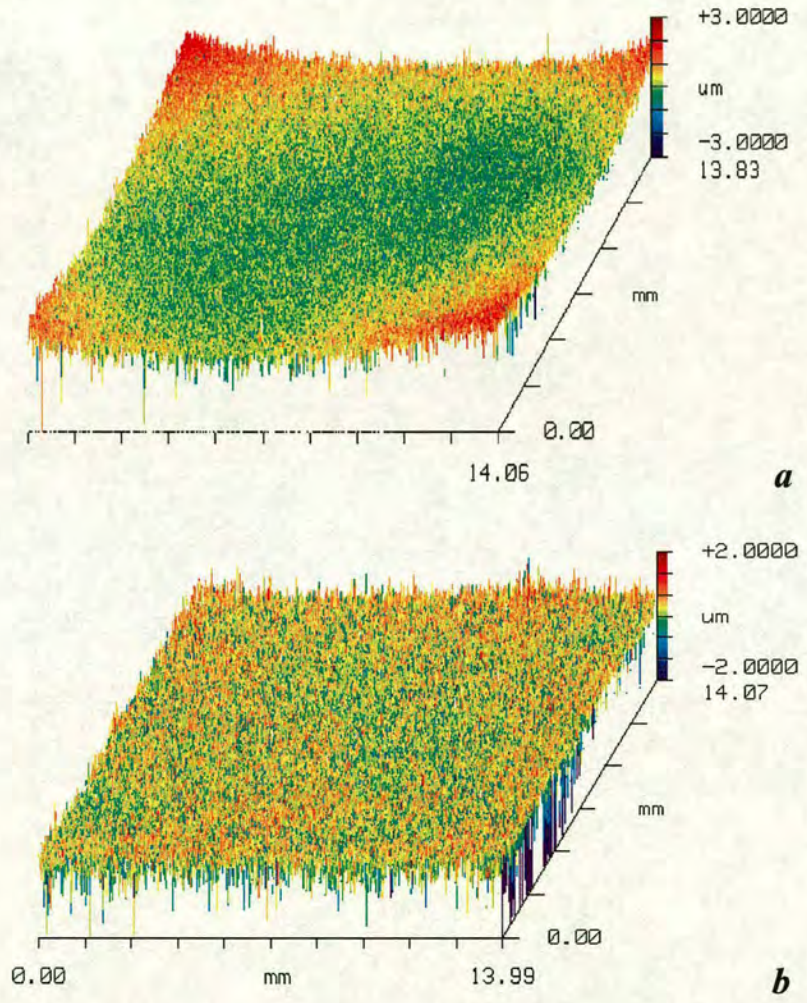


Figure 10.1 White light interferogram images of 512 device before, *a*, and after, *b*, circuitry has been removed

The compensating films thickness/stress can be tuned to 'cancel-out' the stress caused by the circuitry. This is currently being investigated and the initial results indicate that it should, indeed, be feasible. As the die bow is the same for all the devices on the entire wafer it should be possible to deposit this compensating film

on the back of the whole wafer. Once the wafers have been diced the back-side film will compensate for the front side circuitry induces stress. This would enable a wafer scale die flattening method to be developed.

10.4.2. Processing

There are several difficulties encountered when using the process steps in the convential way, the main ones are listed below:

1. The inability to measure the oxide thickness remaining over the array after CMP (due to a multi-dielectric layer, passiviation/SiO_2)
2. Difficulty in etching vias because of multi-dielectric layer passiviation/SiO_2
3. Difficulty in etching vias because of their depth of $\approx 1\mu m$ passivation and an unknown thickness of SiO_2
4. The necessity to perform two separate CMP steps (the first to planarise the circuitry the second to planarise the light blocking layer)

All these problems can be reduced if the process flow order is modified, Table 10-1

By modifying the processing order certain advantages can be made:

1. The first via etch is through the passivation which is of know thickness
2. Once the light blocking metal has been deposited the entire array can then be planarised, resulting in only one CMP step. It also has the added advantage that the SiO_2 over the array can now be measured, aiding via etching.
3. The light blocking layer is no longer planarised removing any possibility of a 'light guide' being made between mirror and blocking layer metals.
4. A reduction in overall via etch depth reducing step coverage concerns

Two 150mm wafers are being processed to evaluate the viability of the modified process flow. A schematic cross section of the device made with the two different process flows can be seen in Figure 10.2 and Figure 10.3.

Conventional Processing	Modified Processing
1. Deposit 4μm ECR PEVCD SiO_2	1. Pattern and etch light blocking layer vias into 1μm Si_xN_x passivation
2. Pattern etch-back window and etch to array 0.8μm step height	2. Deposit 1μm aluminium for light blocking layer
3. CMP	3. Pattern and etch light blocking layer
4. Pattern light blocking layers vias and etch through ?μm SiO_2 and 1μm Si_xN_x passivation	4. Deposit 4μm ECR PEVCD SiO_2
5. Deposit 1μm aluminium for light blocking layer	5. Pattern etch-back window and etch to 0.8μm array step height
6. Pattern and etch light blocking layer	**6. CMP**
7. Deposit 2μm SiO_2	7. Pattern mirror via and etch through 1μm SiO_2
8. Pattern etch-back window and etch to 0.8μm(?) array step height	8. Fill vias
9. CMP	9. Damascene vias
10. Pattern mirror via and etch	10. Deposit 100nm aluminium mirror metal
11. Fill vias	11. Pattern and etch mirrors
12. Damascene vias	
13. Deposit 100nm aluminium mirror metal	
14. Pattern and etch mirrors	

Table 10-1 Comparison of two different processing methods

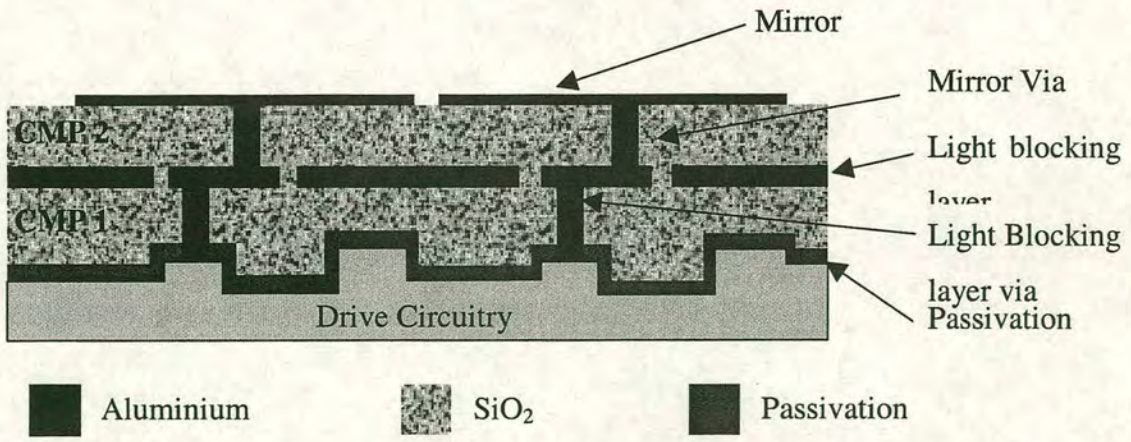


Figure 10.2 Schematic cross-section of 2 mirrors using conventional processing route

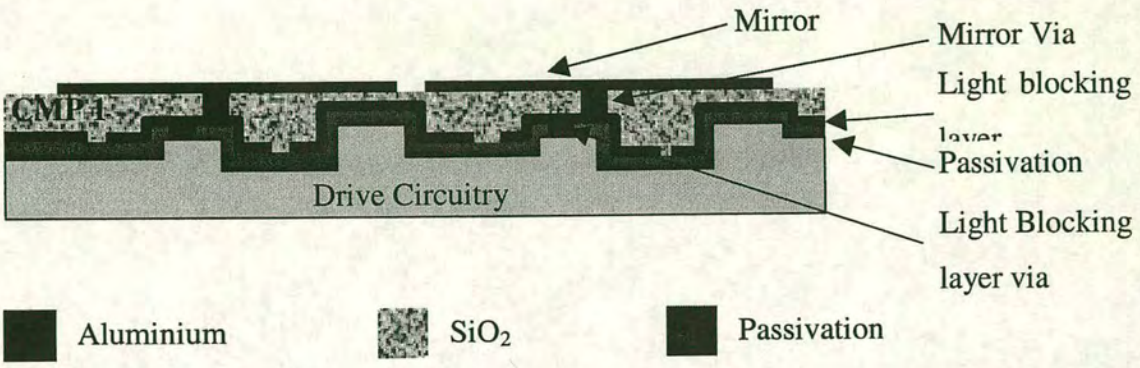


Figure 10.3 Schematic cross-section of 2 mirrors using the modified processing route

10.5. Final Comments

I have investigated various CMP methodologies for the improvement of LCoS SLM devices. These include both dielectric and metal planarisation techniques. For dielectric CMP it was necessary to devise a novel pre-CMP etch to remove the phenomenon of array doming. With the implementation of this technique array doming has been completely removed producing a flat featureless device surface.

Building on this improvement I then developed a via damascene technique. This produces vias which were level with the dielectric surface, which allows the deposition of thin, highly specular mirrors. Further to this, it allowed the use of a novel planarisation method using a lift-off technique. The total elimination of all backplane surface topography vastly improved the LC fill dynamics

11. Appendix

APPENDIX A

Metrology

To accurately assess the results of any experiment, it is essential to have access to adequate metrology equipment. Listed below are the main pieces of equipment I have used during my Ph.D.

Thin Film Measurement

The thin film measuring gauge used was a Nanoscope Model 010-180. The range of the Nanoscope is 0μm to ≈4μm for SiO_2 on silicon and 0.5μm to 2μm for SiO_2 on aluminium. Unfortunately one of the biggest drawbacks with this instrument is its inability to measure multi-film stacks, making it impossible to measure the SiO_2 remaining, after CMP on a product wafer. This is because the device, apart from the bondpads, is covered with some form of passivation (silicon nitride) making direct measurement of SiO_2 remaining after CMP impossible. The only method to asses SiO_2 thickness is by measuring the remaining SiO2 over the bondpads, and using the pre-CMP step-heights to calculate SiO_2 thickness remaining over the array area.

Scanning Electron Microscope

The scanning electron microscope (SEM) has been used extensively in the preparation of images for this thesis. The SEM used is located in the geology department and is a Philips model XL30CP.

Surface Profilometery

Dektak

Throughout the metal CMP trials the Dektak was used to assess the amount of dishing and erosion induced by the CMP process. Unlike the CMP of SiO_2, which is concerned mainly with step heights, metal polishing deals with 'trench' depths.

Profilometers have excellent height sensitivity, but can have relatively poor lateral resolution. The limit of the lateral resolution is a function of stylus size and configuration used. The Dektak the stylus radius is in the order of 2 to 3 microns.

When the tip traverses the surface the profile generated is not an exact match to the feature being measured, Figure 11.1. In extreme cases the resulting profile trace is far removed from that of the feature being measured, Figure 11.2.

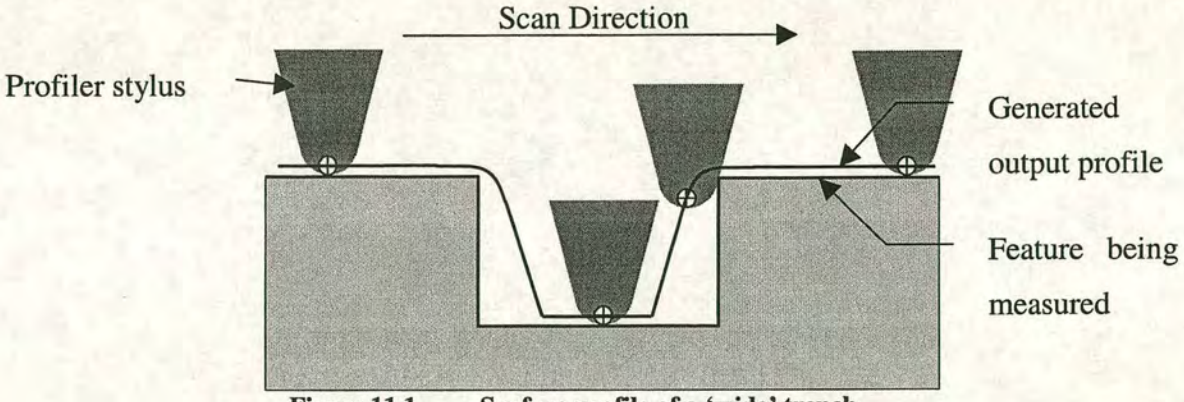


Figure 11.1 Surface profile of a 'wide' trench

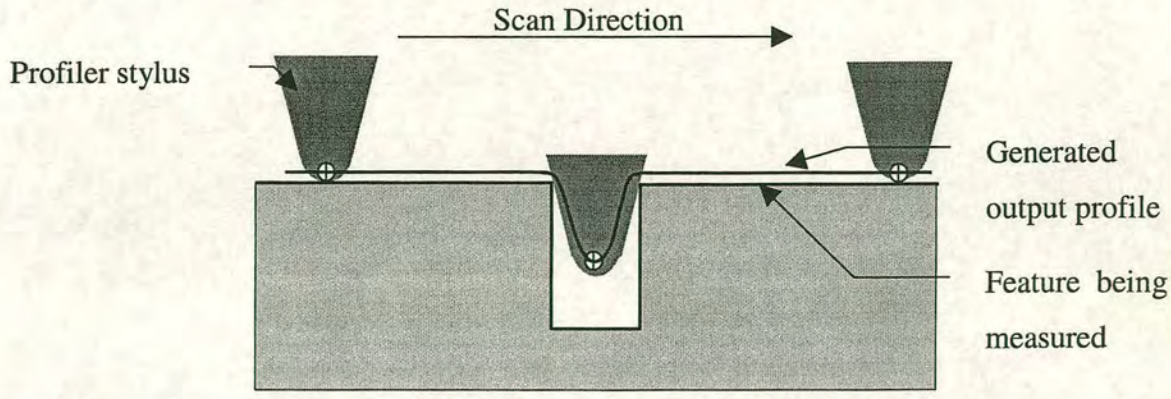


Figure 11.2 Surface profile of a 'narrow' trench

The maximum stylus penetration depth for a given feature size can be calculated using Equation 11-1

$$d \geq 2\pi\sqrt{hr}$$

Equation 11-1 Relationship between stylus radius and lateral resolution[129]

Where ***d*** *is separation of surface features*

r *is the stylus radius and*

h *is the feature depth*

The damascene test pattern (Chapter 6) contained features from 25μm to 1μm in width, with spacing ranging from 30μm down to 4μm. As such, it was thought that features less than 4μm in width may not be resolved to their full depth using the 5μm diameter stylus.

Other considerations to be taken into account when performing a surface profile trace are stylus force and speed. If the force on the stylus is too high it will damage the surface, if the speed is too high it will cause the stylus to bounce over the surface. A compromise has to be made between the two, taking into account the dimensions of the feature being measured. A low stylus force, 2μg, coupled with a scan speed of $3\mu s^{-1}$ was generally used.

Atomic Force Microscope (AFM)

When dealing with surface finishes or very small features (e.g. 2μm vias) the Dektak becomes unusable because of its relatively large stylus radii. The use of an atomic force microscope (AFM) makes it possible to investigate surface finishes on the nanometer scale (both vertically and laterally) and is essential for the analysis of CMP performance for damascened vias. The AFM used throughout this study was a Digital Instruments model D5000.

The lateral resolution situation with the AFM is somewhat more complicated than the Dektak. The Dektaks tip, although not particularly small, is at least symmetrical. The AFM tip, due to its manufacturing technique, is asymmetrical in shape, Figure 11.3

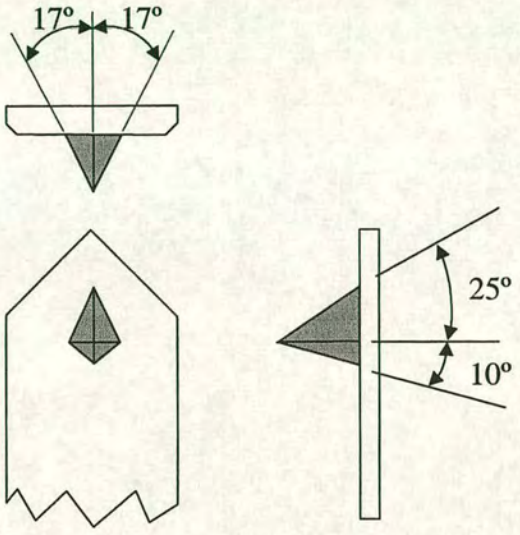


Figure 11.3 AFM stylus configuration theoretical tip shape[130]

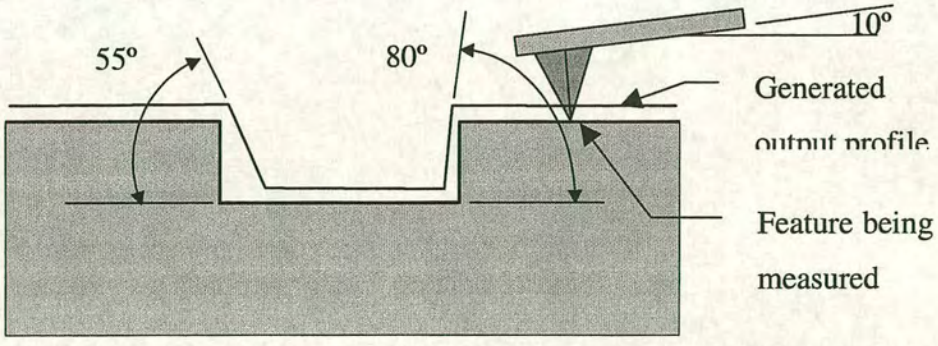


Figure 11.4 AFM probe tip profile artefact

This asymmetry results in different scan profiles depending which part of the tip is used for imaging the sample, Figure 11.4. This is of more concern when dealing with 'large' step heights than with the smooth features on polished

samples. It should, however always be kept in mind when any analysis of the images is performed.

Zygo White Light Interferometer

For large scale surface morphology studies, especially in the investigation of die bow/warp, a 'Zygo' was used. This is a scanning white-light interferometer capable of nanometer vertical resolution. To increase the size of the sample area a computer controlled motorised stage is used to position the sample and sample image stitching software is used to increase the maximum sample image size.

The Zygo white-light interferometry uses a traditional technique in which a pattern of bright and dark lines (fringes) result from an optical path difference, between a reference and a sample beam. Incoming light is split inside an interferometer, one beam going to an internal reference surface and the other to the sample, Figure 11.5. After reflection, the beams recombine inside the interferometer, undergoing constructive and destructive interference and producing the light and dark fringe pattern. A precision vertical scanning transducer and camera together generate a three-dimensional interferogram of the surface, processed by the resulting in a quantitative 3-D image.

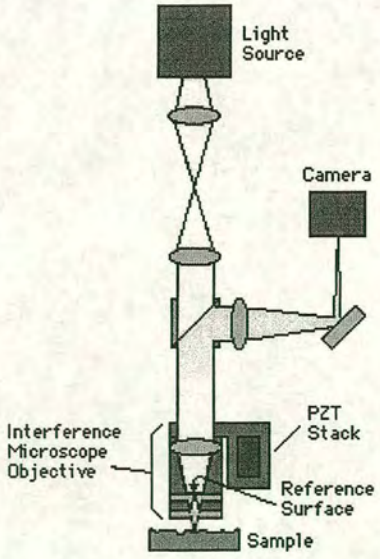


Figure 11.5 Schematic of Zygo White Light Interferometer operation

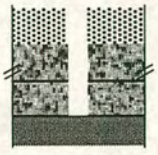
APPENDIX B

Dual Damascene Methodologies

In the mirror damascene technicue there is a choice to be made: whether to define the via or the mirror first[131].

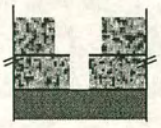
Via First

1.Deposition of a thick dielectric (the thickness is tailored to include both line and via dielectric). A thin etch stop layer can be included. Multi-step dielectric deposition allows for different k values for line and via dielectrics.

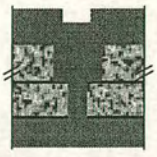


2.Via pattern is etched through the entire dielectric stack.

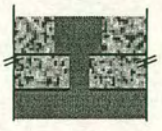
3.Photoresist processing for trench pattern. Use the buried etch stop to terminate the trench etch.



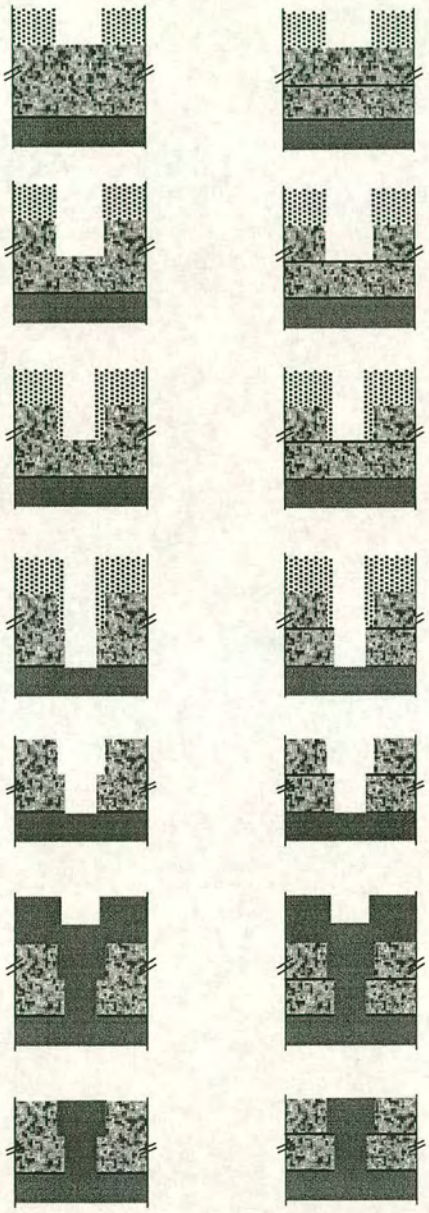
4.Trench etch terminates on the buried etch stop.



5.Photoresist removal. Finished damascene structure.



Improved with stop layer



1.Deposition of a thick dielectric (the thickness is tailored to include both line and via dielectric).

2.Line pattern is etched in the dielectric.

3.Photoresist processing for via pattern.

4.Via pattern is etched in the dielectric.

5.Photoresist removal.

Advantages and Disadvantages

	Line First	Via First
Advantages	Optimize the etch processes separately. One step thick dielectric deposition. Greater flexibility for dielectric depositions (multi-layer materials with different k values).	Buried etch stop allows use of low-k material for line dielectric. Optimize the dielectric etch for line and via separately. More tolerance to misalignment of line to via.
Disadvantages	Timed etch for the line required. Line etch parameters critical (uniformity, etchrate drift). Difficult to implement a multi-dielectricstructure (different etch selectivities for different dielectric composition). Line dimensions must be bigger than via dimensions.	Deep via etch is more difficult. Removal of resist at the bottom of the via is difficult. Higher selectivity to buried etch stop is required (buried etch stop is typically Silicon Nitride).

All the dual-damascene processing carried out in this study used the line (mirror) first method, without a hard stop layer. This method was chosen because it was found that, because of the relatively large mirror size (18μm x 18μm), no

disruption in the photoresist thickness was evident at the mirror trench bottom after coating. This made the patterning of the vias no more problematic then if the were patterned on a smooth surface.

The absence of a stop layer (omitted to simplify processing) meant that the mirror depth was determined by a timed etch cycle. This method did not appear to cause any processing problems.

APPENDIX C

Process Flow For Optimised Post-Processing of LCoS SLMs

1. Resist coat and pattern with light blocking layer via (via 1)
2. Etch vias through passivating silicon nitride
3. Remove resist
4. Subject wafer to 15 minutes argon atom bombardment (pre-sputter clean)
5. Sputter 1.5μm aluminium (Metal 1)
6. Resist coat and pattern light blocking layer (Metal 1)
7. Deposit 3μm ECR PEVCD SiO_2
8. Pattern etch-back window
9. Etch to produce an array step height of ≈0.8μm
10. Remove resist
11. CMP
12. Resist coat and pattern with mirror vias (via 2)
13. Etch vias
14. Subject wafer to 15 minutes argon atom bombardment (pre-sputter clean)
15. Sputter 1.5μm aluminium
16. Damascene vias
17. SiO_2 buff
18. Subject wafer to 20 minutes argon atom bombardment as pre-sputter clean
19. Sputter 0.1μm aluminium mirror metal (metal 2)
20. Deposit 0.8μm ECR PEVCD SiO_2 (for spacers)
21. Resist coat and pattern spacers
22. Etch SiO_2 spacers using metal 2 as a stop layer
23. Resist coat and pattern mirrors (metal 2)
24. Etch mirrors
25. Deposit 0.1μm SiO_2
26. Remove SiO_2 overburden and resist
27. Resist coat
28. Dice

APPENDIX D

Clean Room Equipment at The University of Edinburgh

Dry Etch

Aluminium

STS load locked aluminium and polysilicon RIE etcher using SiCl4, and Cl2 chemistry (3-6 inch wafers).

Silicon Dioxide

Plasmatherm PK244O RIE system using Fluorine chemistry to anisotropically etch silicon dioxide and nitride from 20 × 3 in wafers/run. It can also be used to etch 4-8 inch wafers.

STS PF 508 barrel reactor for plasma ashing of photoresist

Deposition

Aluminium

Balzers BAS450 coater system with two 5 in × 10 inch targets presently used for coating up to 24 × 3 inch wafers with Al/1%Si, Al, W and Ti. It is also capable of coating 4 and 6 inch wafers. Ion beam pre-cleaning is available using an Ion Tec Inc Kaufmann source.

Silicon Dioxide

Oxford Plasma Technology ECR deposition of SiO2 and Nitride. (3-6 inch wafers)

11. Appendix

APPENDIX A

Metrology

To accurately assess the results of any experiment, it is essential to have access to adequate metrology equipment. Listed below are the main pieces of equipment I have used during my Ph.D.

Thin Film Measurement

The thin film measuring gauge used was a Nanoscope Model 010-180. The range of the Nanoscope is 0μm to ≈4μm for SiO_2 on silicon and 0.5μm to 2μm for SiO_2 on aluminium. Unfortunately one of the biggest drawbacks with this instrument is its inability to measure multi-film stacks, making it impossible to measure the SiO_2 remaining, after CMP on a product wafer. This is because the device, apart from the bondpads, is covered with some form of passivation (silicon nitride) making direct measurement of SiO_2 remaining after CMP impossible. The only method to asses SiO_2 thickness is by measuring the remaining SiO2 over the bondpads, and using the pre-CMP step-heights to calculate SiO_2 thickness remaining over the array area.

Scanning Electron Microscope

The scanning electron microscope (SEM) has been used extensively in the preparation of images for this thesis. The SEM used is located in the geology department and is a Philips model XL30CP.

Surface Profilometery

Dektak

Throughout the metal CMP trials the Dektak was used to assess the amount of dishing and erosion induced by the CMP process. Unlike the CMP of SiO_2, which is concerned mainly with step heights, metal polishing deals with 'trench' depths.

Profilometers have excellent height sensitivity, but can have relatively poor lateral resolution. The limit of the lateral resolution is a function of stylus size and configuration used. The Dektak the stylus radius is in the order of 2 to 3 microns.

When the tip traverses the surface the profile generated is not an exact match to the feature being measured, Figure 11.1. In extreme cases the resulting profile trace is far removed from that of the feature being measured, Figure 11.2.

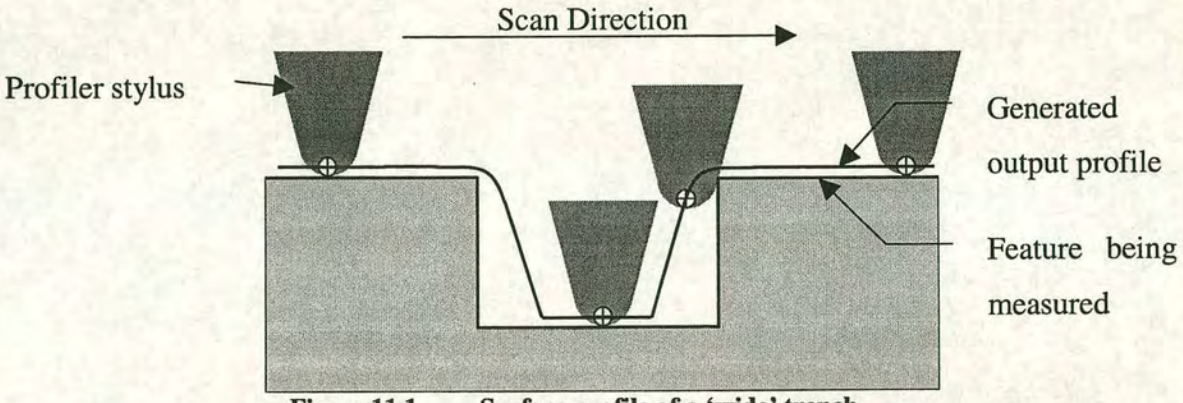


Figure 11.1 Surface profile of a 'wide' trench

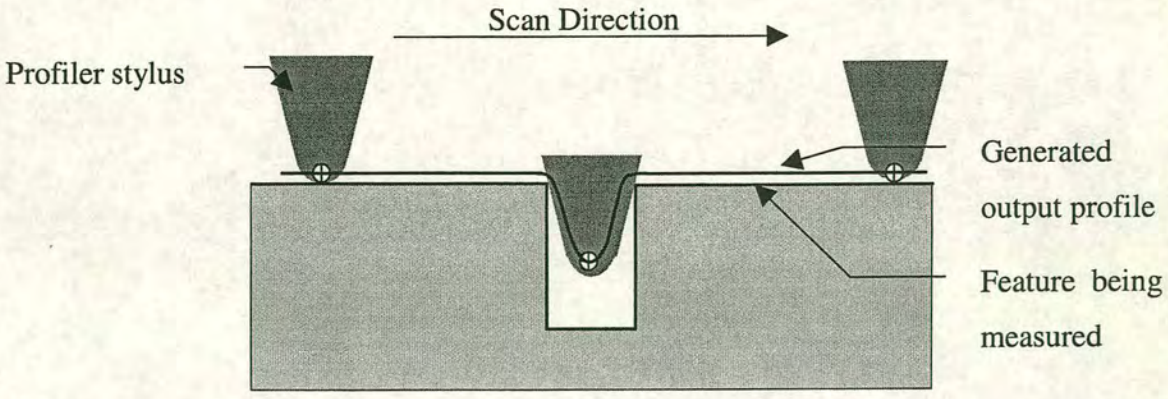


Figure 11.2 Surface profile of a 'narrow' trench

The maximum stylus penetration depth for a given feature size can be calculated using Equation 11-1

$$d \geq 2\pi\sqrt{hr}$$

Equation 11-1 Relationship between stylus radius and lateral resolution[129]

Where ***d*** *is separation of surface features*

r *is the stylus radius and*

h *is the feature depth*

The damascene test pattern (Chapter 6) contained features from 25μm to 1μm in width, with spacing ranging from 30μm down to 4μm. As such, it was thought that features less than 4μm in width may not be resolved to their full depth using the 5μm diameter stylus.

Other considerations to be taken into account when performing a surface profile trace are stylus force and speed. If the force on the stylus is too high it will damage the surface, if the speed is too high it will cause the stylus to bounce over the surface. A compromise has to be made between the two, taking into account the dimensions of the feature being measured. A low stylus force, 2μg, coupled with a scan speed of $3\mu s^{-1}$ was generally used.

Atomic Force Microscope (AFM)

When dealing with surface finishes or very small features (e.g. 2μm vias) the Dektak becomes unusable because of its relatively large stylus radii. The use of an atomic force microscope (AFM) makes it possible to investigate surface finishes on the nanometer scale (both vertically and laterally) and is essential for the analysis of CMP performance for damascened vias. The AFM used throughout this study was a Digital Instruments model D5000.

The lateral resolution situation with the AFM is somewhat more complicated than the Dektak. The Dektaks tip, although not particularly small, is at least symmetrical. The AFM tip, due to its manufacturing technique, is asymmetrical in shape, Figure 11.3

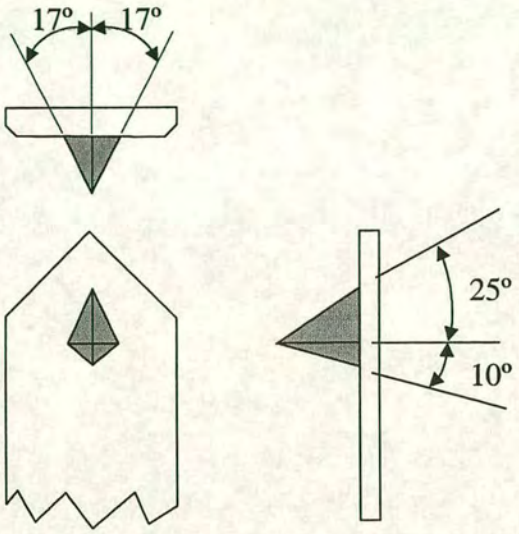


Figure 11.3 AFM stylus configuration theoretical tip shape[130]

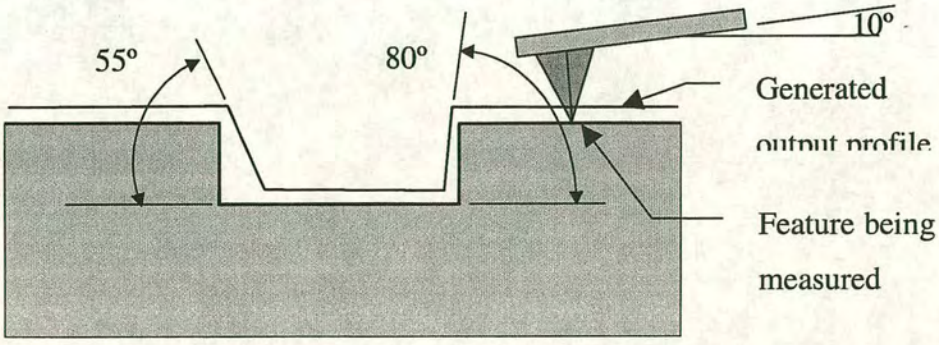


Figure 11.4 AFM probe tip profile artefact

This asymmetry results in different scan profiles depending which part of the tip is used for imaging the sample, Figure 11.4. This is of more concern when dealing with 'large' step heights than with the smooth features on polished

samples. It should, however always be kept in mind when any analysis of the images is performed.

Zygo White Light Interferometer

For large scale surface morphology studies, especially in the investigation of die bow/warp, a 'Zygo' was used. This is a scanning white-light interferometer capable of nanometer vertical resolution. To increase the size of the sample area a computer controlled motorised stage is used to position the sample and sample image stitching software is used to increase the maximum sample image size.

The Zygo white-light interferometry uses a traditional technique in which a pattern of bright and dark lines (fringes) result from an optical path difference, between a reference and a sample beam. Incoming light is split inside an interferometer, one beam going to an internal reference surface and the other to the sample, Figure 11.5. After reflection, the beams recombine inside the interferometer, undergoing constructive and destructive interference and producing the light and dark fringe pattern. A precision vertical scanning transducer and camera together generate a three-dimensional interferogram of the surface, processed by the resulting in a quantitative 3-D image.

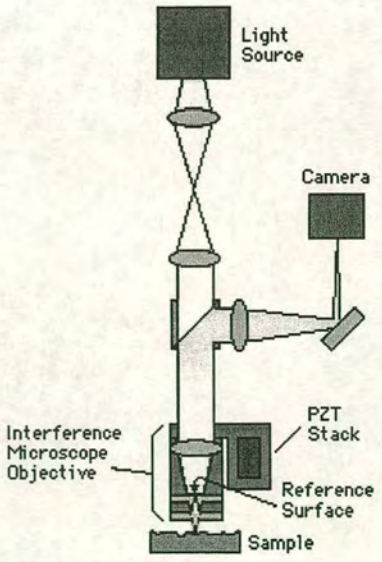


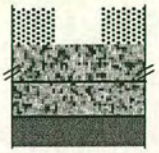
Figure 11.5 Schematic of Zygo White Light Interferometer operation

APPENDIX B

Dual Damascene Methodologies

In the mirror damascene technicue there is a choice to be made: whether to define the via or the mirror first[131].

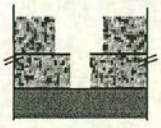
Via First



1.Deposition of a thick dielectric (the thickness is tailored to include both line and via dielectric). A thin etch stop layer can be included. Multi-step dielectric deposition allows for different k values for line and via dielectrics.

2.Via pattern is etched through the entire dielectric stack.

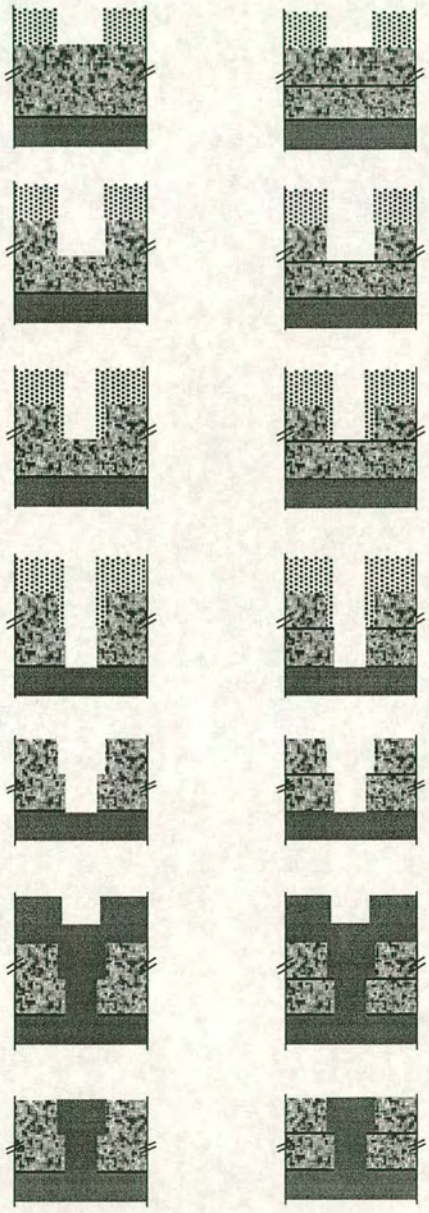
3.Photoresist processing for trench pattern. Use the buried etch stop to terminate the trench etch.



4.Trench etch terminates on the buried etch stop.

5.Photoresist removal. Finished damascene structure.

Improved with stop layer



1.Deposition of a thick dielectric (the thickness is tailored to include both line and via dielectric).

2.Line pattern is etched in the dielectric.

3.Photoresist processing for via pattern.

4.Via pattern is etched in the dielectric.

5.Photoresist removal.

Advantages and Disadvantages

	Line First	Via First
Advantages	Optimize the etch processes separately. One step thick dielectric deposition. Greater flexibility for dielectric depositions (multi-layer materials with different k values).	Buried etch stop allows use of low-k material for line dielectric. Optimize the dielectric etch for line and via separately. More tolerance to misalignment of line to via.
Disadvantages	Timed etch for the line required. Line etch parameters critical (uniformity, etchrate drift). Difficult to implement a multi-dielectricstructure (different etch selectivities for different dielectric composition). Line dimensions must be bigger than via dimensions.	Deep via etch is more difficult. Removal of resist at the bottom of the via is difficult. Higher selectivity to buried etch stop is required (buried etch stop is typically Silicon Nitride).

All the dual-damascene processing carried out in this study used the line (mirror) first method, without a hard stop layer. This method was chosen because it was found that, because of the relatively large mirror size (18μm x 18μm), no

disruption in the photoresist thickness was evident at the mirror trench bottom after coating. This made the patterning of the vias no more problematic then if the were patterned on a smooth surface.

The absence of a stop layer (omitted to simplify processing) meant that the mirror depth was determined by a timed etch cycle. This method did not appear to cause any processing problems.

APPENDIX C

Process Flow For Optimised Post-Processing of LCoS SLMs

1. Resist coat and pattern with light blocking layer via (via 1)
2. Etch vias through passivating silicon nitride
3. Remove resist
4. Subject wafer to 15 minutes argon atom bombardment (pre-sputter clean)
5. Sputter 1.5μm aluminium (Metal 1)
6. Resist coat and pattern light blocking layer (Metal 1)
7. Deposit 3μm ECR PEVCD SiO_2
8. Pattern etch-back window
9. Etch to produce an array step height of ≈0.8μm
10. Remove resist
11. CMP
12. Resist coat and pattern with mirror vias (via 2)
13. Etch vias
14. Subject wafer to 15 minutes argon atom bombardment (pre-sputter clean)
15. Sputter 1.5μm aluminium
16. Damascene vias
17. SiO_2 buff
18. Subject wafer to 20 minutes argon atom bombardment as pre-sputter clean
19. Sputter 0.1μm aluminium mirror metal (metal 2)
20. Deposit 0.8μm ECR PEVCD SiO_2 (for spacers)
21. Resist coat and pattern spacers
22. Etch SiO_2 spacers using metal 2 as a stop layer
23. Resist coat and pattern mirrors (metal 2)
24. Etch mirrors
25. Deposit 0.1μm SiO_2
26. Remove SiO_2 overburden and resist
27. Resist coat
28. Dice

APPENDIX D

Clean Room Equipment at The University of Edinburgh

Dry Etch

Aluminium

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Silicon Dioxide

Oxford Plasma Technology ECR deposition of SiO2 and Nitride. (3-6 inch wafers)

Wafer Lithography

Photoresist coating, developing and baking are achieved on 3" and 6" wafers on two SVG 8600 track systems, each comprising:

Printing

Optimetrix 8010, g-line, 0.32 NA, (3") 10X reduction stepper with 1.0 micron resolution over 1 cm square field and die by die alignment to ±0.3 micron.

Optimetrix 8605, g-line, 0.32 NA, (3, 4 & 6") 5X reduction stepper with 1.0 micron resolution over 1.4 cm square field and die by die alignment to ±0.3 micron.

Chemical Mechanical Polishing (CMP)

Presi Mecapol E460 polisher configured for 3-8 inch wafers.

SVG 8600 series double sided 6 inch scrubber.

APPENDIX E

Publications

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